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A digital automatic frequency control design.

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A DIGITAL AUTOMATIC FREQUENCY CONTROL DESIGN

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THESIS

A DIGITAL AUTOMATIC FREQUENCY CONTROL DESIGN

by

Glenn Everette Ewing

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This paper describes a digital automatic frequency control (AFC) system designed for use with almost any conventionally-tuned, high-frequency communications equipment. When connected to a high-quality equipment, such as an R-390 receiver, frequency accuracy and stability approaching that of frequency synthesizers can be obtained.

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frequency-determining oscillators in the controlled equipment, computes and displays the operating frequency to the nearest Hertz. When the AFC is engaged, any deviation of the computed operating frequency from the desired frequency causes an error correction voltage to be generated. Use of this system requires that the controlled equipment be modified for voltage trimming of the tuning oscillator.

A Digital Automatic Frequency Control Design

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ABSTRACT

This paper describes a digital automatic frequency control (AFC) system designed for use with almost any conventionally-tuned, high-frequency communications equipment. When connected to a high-quality equipment, such as an R-390 receiver, frequency accuracy and stability approaching that of frequency synthesizers can be obtained.

The AFC system digitally counts the frequency of all frequency-determining oscillators in the controlled equipment, computes and displays the operating frequency to the nearest Hertz. When the AFC is engaged, any deviation of the computed operating frequency from the desired frequency causes an error correction voltage to be generated. Use of this system requires that the controlled equipment be modified for voltage trimming of the tuning oscillator.

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LIST OF DRAWINGS

TABLE I. Abbreviations Used in Drawings

CTR	Counter
CUR	Current
DN	Down
G1.00	1.00-second gate
G1.02	1.02-second gate
H	Logical high
L	Lock
LP	Lock pulse
LPB	Lock pushbutton
MEAS	Measurement
OSC	Oscillator
P1, P2, etc.	Sequencing pulses
PCC	Primary counter clear
PDN	Primary counter down input
PLL	Primary latch load
PRI	Primary
PUP	Primary counter up input
SCC	Secondary counter clear
SCL	Secondary counter load
SDN	Secondary counter down input
SEC	Secondary
SLL	Secondary latch load
SSMV	Single shot multi-vibrator
UL	Unlock
ULPB	Unlock pushbutton

I. INTRODUCTION

Some modern high-frequency communications systems require frequency accuracy and long-term frequency stability beyond the performance capabilities of conventionally-tuned (non-synthesized) equipment. For example, digital data and multiplexed radioteletype communications require frequency accuracies within a few Hertz and long-term stability which maintains this accuracy indefinitely. While not as demanding, single-sideband systems require absolute accuracies within a few tens of Hertz, which can be accomplished with the best conventionally-tuned equipment only if it is periodically retuned. Applications such as signal intercept intelligence gathering can be improved by a direct frequency readout which is more accurate than the indirect frequency calibration available on conventionally-tuned communications equipment.

Recent advancements in digital integrated circuit technology have resulted in improved and more economical frequency synthesizer designs and most of the military and commercial high-frequency communications equipment now being produced is frequency synthesized. There are still large numbers of high quality, conventionally-tuned communications equipment in service. Their useful lifetime could be extended significantly if their frequency accuracy and

stability performance were improved to satisfy current and future requirements.

The digital automatic frequency control (AFC) system described in this paper is intended for retrofit on existing, conventionally-tuned, high-frequency communications equipment. When used on good quality equipment, it is intended to improve accuracy and long-term stability to nearly that of frequency synthesized equipment. In addition to its control function, it provides an accurate digital readout of the operating frequency. It can be programmed to work with equipment using almost any hetrodyne scheme employing up to five oscillators.

The system has two modes of operation. In the unlocked mode it measures and displays the current operating frequency but does not otherwise affect equipment operation. In the locked mode the system measures the operating frequency, then generates corrections to reduce any deviation from the desired frequency. The last frequency measured in the unlocked mode is the "desired frequency."

The primary design objectives were to obtain significantly improved performance with a simple AFC system and to keep required equipment modifications to a minimum. Additionally, the system was to be usable with as wide a spectrum of equipment designs as possible.

II. DESIGN DEVELOPMENT

The design of this AFC system was patterned after the phase locked loop (PLL) system used in many modern frequency synthesizers. There are, however, some significant differences in these systems and for this reason this description will be developed without reference to the PLL system. In the following description positive logic will be used. Some of the devices actually used employ negative logic at their inputs and/or outputs but for the sake of clarity this preliminary description will ignore this minor complication. The following notation convention will be observed. All actual frequencies will be noted by lower case symbols, e.g., f_o. The numerical results of corresponding frequency measurements will be noted by upper case symbols.

Table I is a listing of the abbreviations and symbols used for the various signals present in the system. Overscored symbols represent "complimented" or "inverted" signals.

The following conventions will be observed in all diagrams. Control signal paths will be represented by light lines. Other signal and serial data paths will be represented by medium lines. Heavy, ticked lines will represent parallel data paths.

A. BASIC APPROACH

Figures 1 and 2 contain block diagrams which show the basic approach originally taken in developing the design. For clarity, this description will initially assume that the AFC system will be used on a simple equipment which employs a single oscillator which oscillates at the operating frequency, e.g., direct conversion receiver. Further, it is assumed that the oscillator has been modified such that it can be voltage-controlled over a small range each side of the operating frequency.

1. Unlocked Mode

In the unlocked mode the system simply measures and displays the operating frequency. This can be accomplished using the conventional frequency counter diagrammed in Figure 1. Initially the counter is cleared to zero. The output of the oscillator is then counted for a one-second period derived from an accurate, crystal-controlled time base. At the end of one second the content of the counter is equal to the average frequency of the oscillator in Hertz. This number is then transferred to the latch for decoding and display and the counter then cleared in preparation for the next count. The latch preserves the measurement for continuous display until the next measurement is completed.

2. Locked Mode

In the locked mode the system must measure the operating frequency, compare this measurement with the

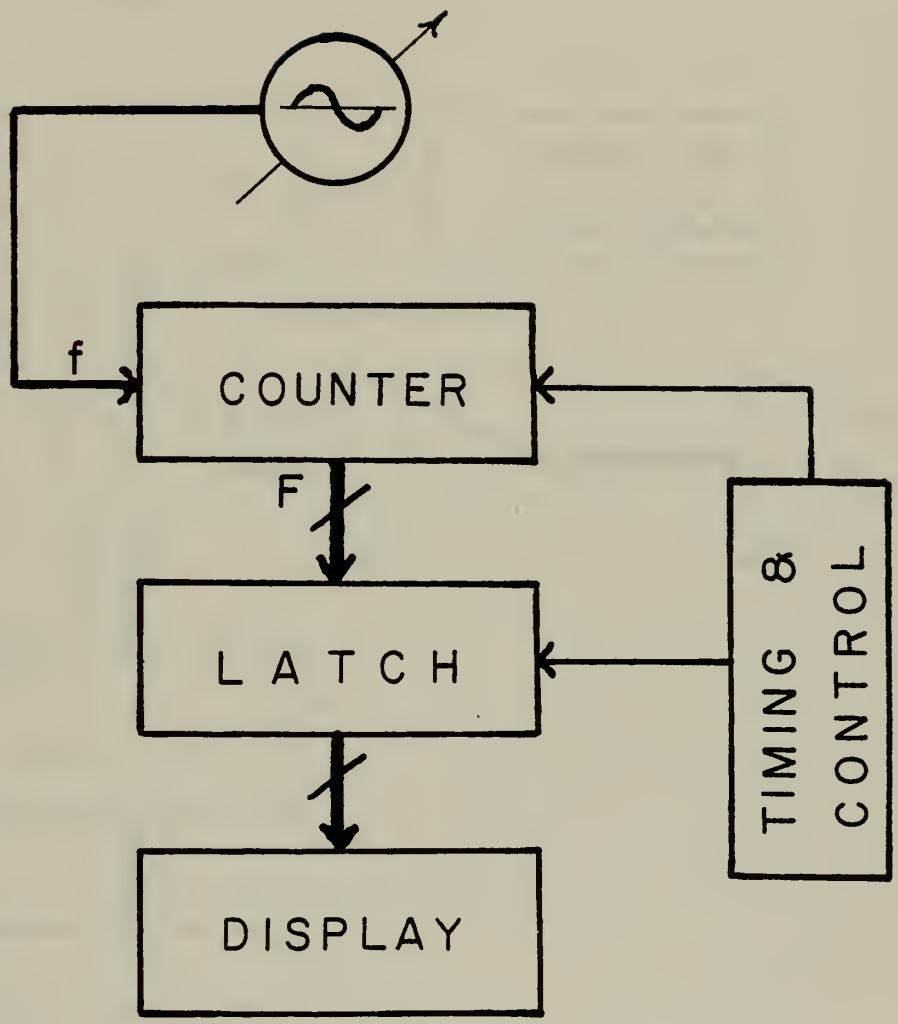


Figure 1 Basic Approach -- Unlocked Mode

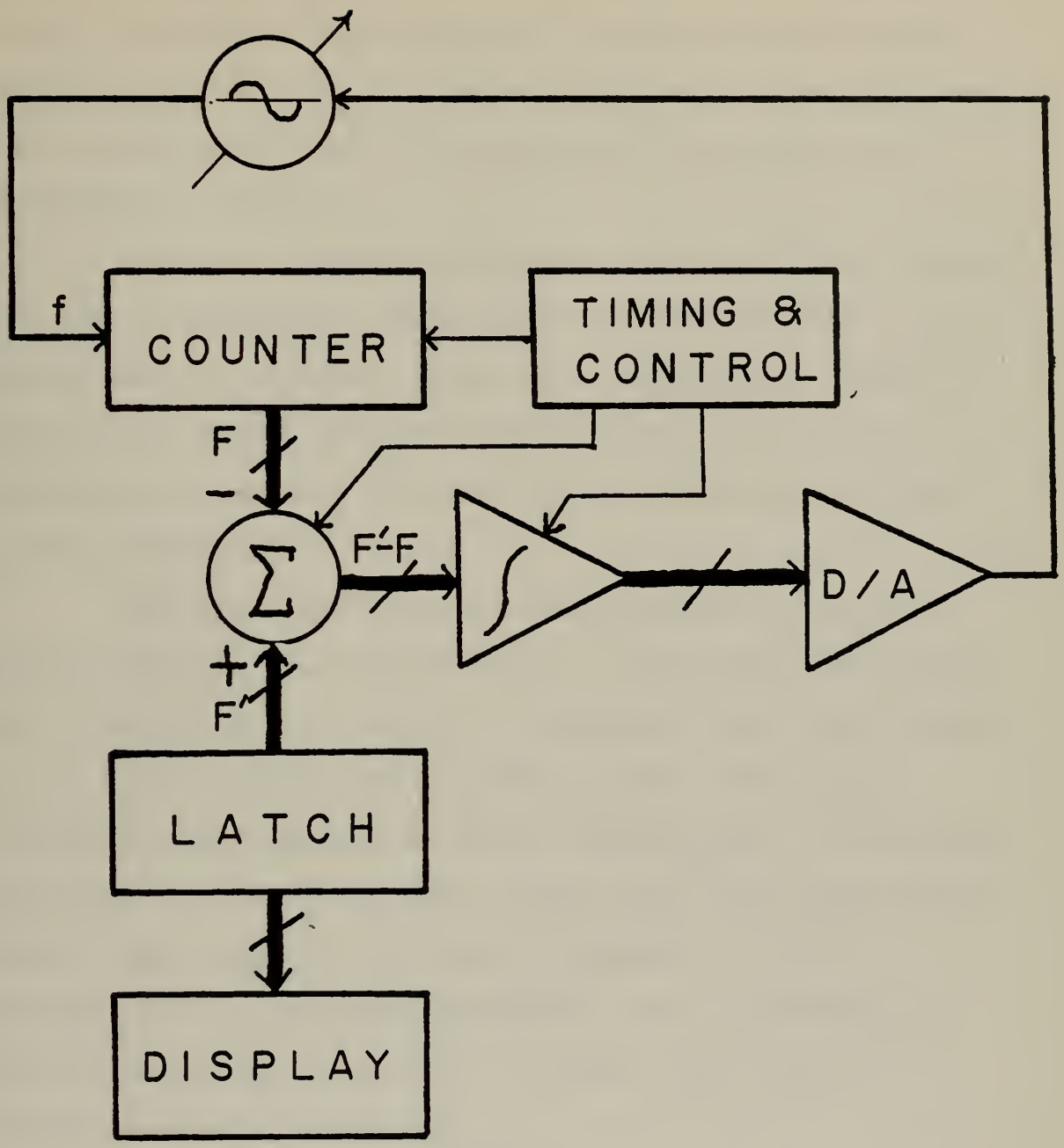


Figure 2 Basic Approach -- Locked Mode

desired frequency, then generate a correction for any detected deviation from the desired frequency. The AFC system, to accomplish this, as originally conceived, is diagrammed in Figure 2.

The last frequency measured in the unlocked mode is the desired frequency. This is stored in the latch when the locked mode is entered. Since this reference is needed as long as the system is in the locked mode, the latch is inhibited from changing its contents as long as the system is in the locked mode.

The operating frequency is measured by the same counter used in the unlocked mode. After each measurement the contents of the counter is subtracted from the contents of the latch to give the frequency error. The control voltage is then shifted an amount proportional to the measured error in the direction to shift the oscillator's frequency back towards the desired frequency. This is accomplished by step-integrating the error measurements and converting the result to a voltage level with a digital-to-analog converter.

3. Multi-Oscillator Provisions

In general, communications receivers have one or more internal oscillators, none of which oscillates at the operating frequency. For example, consider the simple, single conversion, superhetrodyne receiver functionally diagrammed in Figure 3. In this example the conversion oscillator operates at a frequency (f_1) which is the sum of

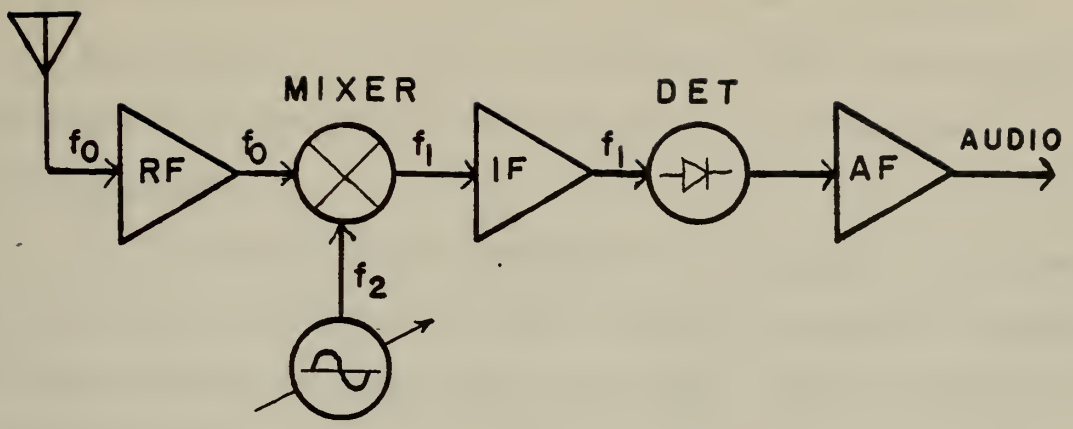


Figure 3 Simple Receiver

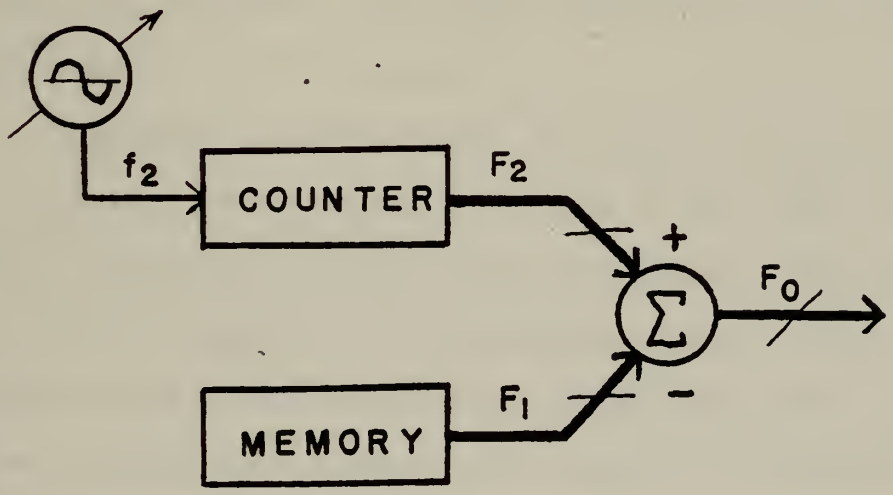


Figure 4 Frequency Measurement and Computation for Simple Reveiver

the operating frequency (f_o) and the center frequency of the IF passband (f_2). This is consistent with the practice of designating communications channels by the channel center frequency.

If the AFC system diagrammed in Figures 1 and 2 was used with this receiver, it would perform as desired except that the conversion oscillator frequency, rather than the operating frequency, would be displayed. Substituting the partial system diagrammed in Figure 4 for the counter in Figures 1 and 2 would correct this discrepancy by computing the operating frequency from the conversion oscillator frequency and the IF frequency.

The receiver diagrammed in Figure 3 would not be able to receive modulation modes such as CW, FSK, SSB, etc., because it does not have the beat frequency oscillator (BFO) usually employed in demodulating these modes. It is important to note that the modulation modes which have the long-term frequency accuracy and stability requirements that originally motivated this project, i.e., FSK and SSB, are among those which are associated with the use of a BFO. For this reason the AFC system design will assume that a BFO is used.

Figure 5 is a functional diagram of the same simple receiver but with a BFO and product detector substituted for the AM detector. The receiver's operating frequency is still determined by the conversion oscillator frequency and the frequency of the center of the IF

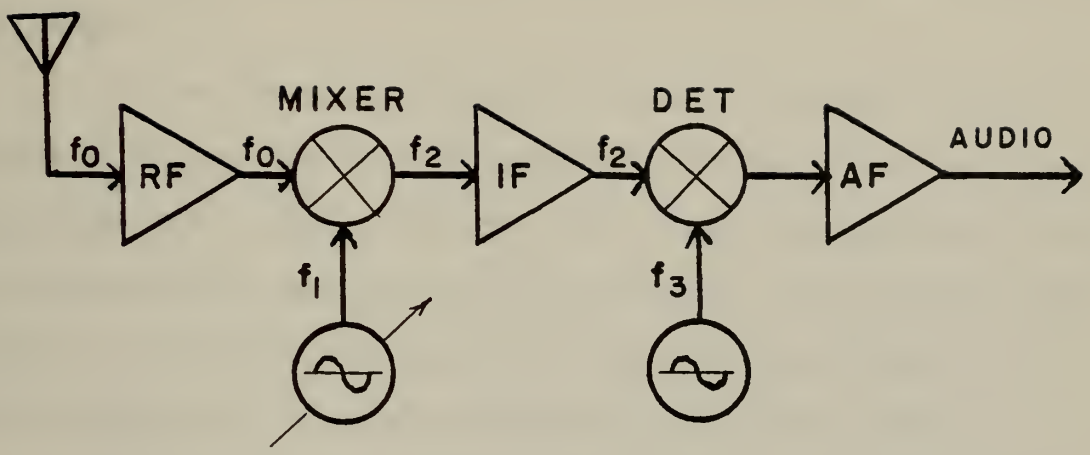


Figure 5 Receiver with BFO

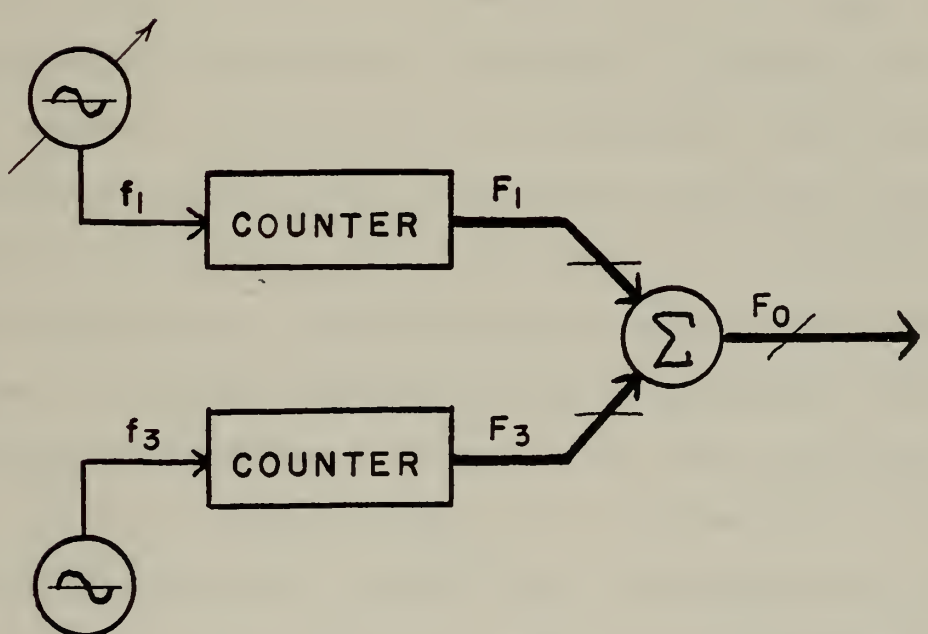


Figure 6 Frequency Measurement and Computation for Receiver with BFO

passband if the "channel center" convention is used. The BFO hetrodynes the IF signal down to audio for amplification and output.

To be tuned properly the received signal must be centered in the receiver's passband and the audio output must have the correct "pitch". The first requirement is met by the accurate setting of the conversion oscillator's frequency. The second is met by the accurate setting of the BFO's frequency for the particular modulation mode.

If the BFO's frequency drifts or otherwise changes slightly the frequencies in the audio output will change by the same absolute amount. However, if, at the same time, the conversion oscillator's frequency is changed by an equal amount in the correct direction and if the change in frequency is small enough to preclude moving any significant portion of the signal out of the passband, the output will remain unaffected. Substituting the partial system diagrammed in Figure 6 for the counter in Figures 1 and 2 takes advantage of this fact. In the locked mode the system would correct for variations in the frequencies of both the conversion oscillator and the BFO. The corrections are always made to the conversion oscillator so changes in the BFO's frequency will cause the signal frequencies to shift relative to the passband. As mentioned above, this can be tolerated if the frequency changes are small enough. However, the possibility of shifting the signal out of the receiver's passband must be considered.

Another effect of using the system as now modified is that the frequency displayed is the "carrier insertion" frequency rather than channel center frequency, i.e., it is equal to the frequency of the oscillator of an equivalent direct conversion receiver. This convention for designating communications channels is sometimes used, especially for SSB, and will be used in this design.

Since this AFC system is intended for use with a wide variety of communications equipments including multi-conversion types, provision must be made for measuring the frequencies of all of the oscillators in any particular hetrodyne scheme and for computing the operating frequency from these measurements. The partial system shown in Figure 7 will accomplish this. Whether a frequency is to be added or subtracted is programmable and must be properly set up when the system is connected to a particular equipment. Thus, by substituting this partial system for the counter in Figures 1 and 2 we have a scheme which should accomplish the desired results.

B. PRELIMINARY CIRCUIT DESIGN

The most obvious approach to designing the circuitry for this system was to implement literally, section by section, the system as shown in Figures 1, 2 and 7, and as described above. This would have been possible but the result would have been far too complex for economical translation into hardware. For example, if the system is to be capable of application to equipment with up to five oscillators, a

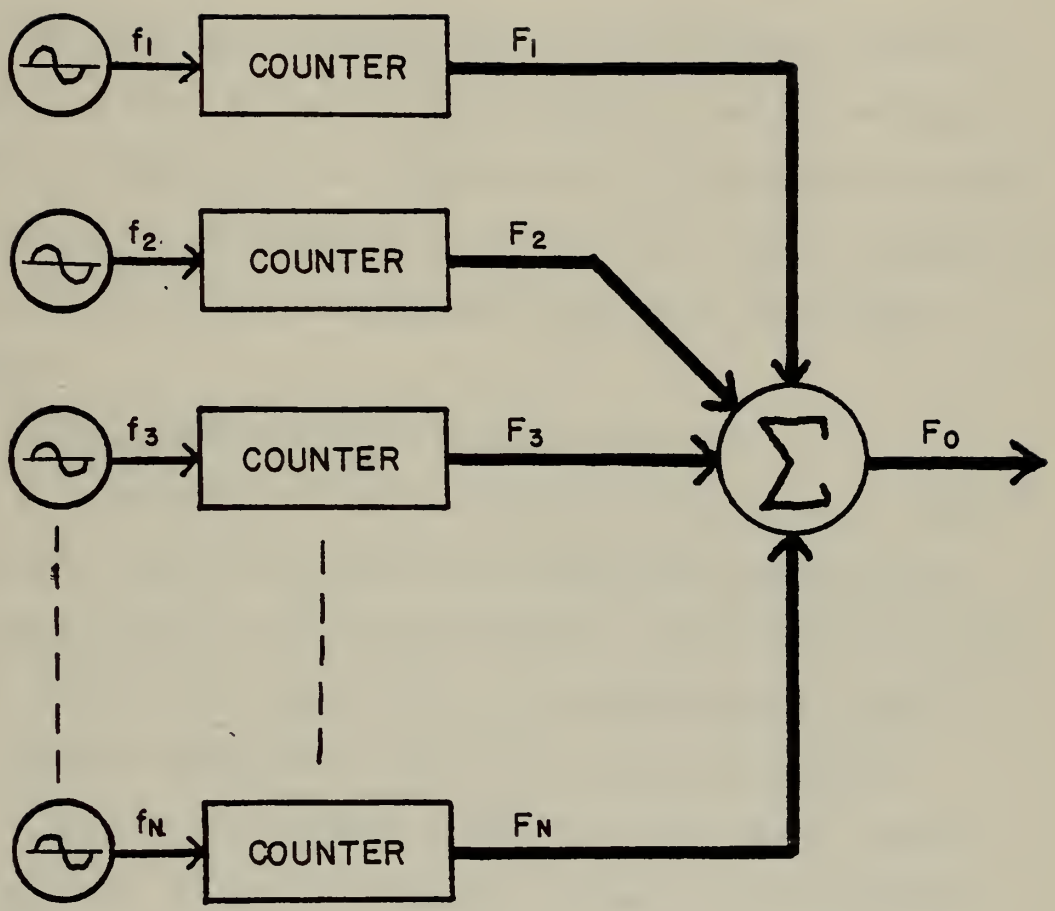


Figure 7 Multi-oscilator Measurement and Computation

literal implementation would require five separate frequency counters and complex circuitry for performing the many additions and subtractions necessary to compute the operating frequency, frequency error, and to perform the integration.

Two factors make considerable simplification possible. The first is that all of the computations can be reduced to a series of additions and subtractions. The second is that in the types of equipment with which the AFC was intended to be used, the internal oscillators have good short-term stability.

1. Programmable Digital Up/Down Counter

A programmable digital up/down counter is a versatile circuit which is capable of combining addition and subtraction with its counting function. This makes it possible to reduce the number of -- or eliminate the need for -- separate adders/subtracters in the AFC system design. Further, by taking advantage of the good, short-term stability of the controlled equipment it is possible to perform all of the counts and computations for measuring the operating frequency and computing the frequency error with a single counter regardless of the number of oscillators involved.

a. Counter Characteristics

A typical up/down counter IC is shown in Figure 8. The contents of the counter can be changed in four different ways. As in a conventional counter, the

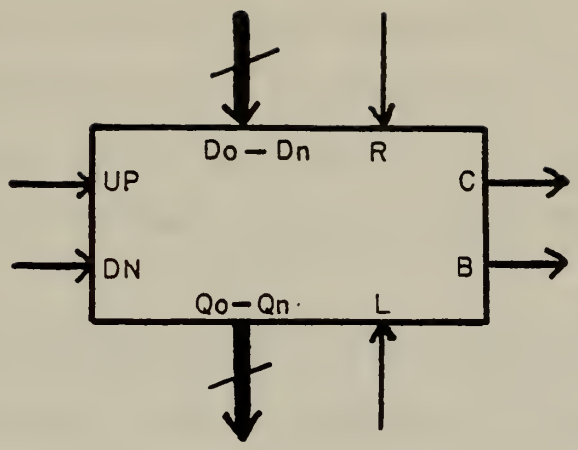


Figure 8 UP/DOWN Counter

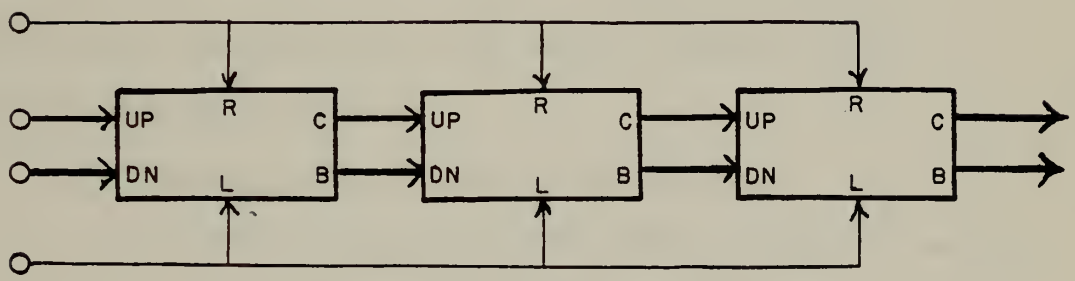


Figure 9 Cascaded Counters

contents can be incremented by strobing the UP input and can be reset to zero by strobing the reset (R) input. Additionally, the contents can be decremented by strobing the down (DN) input and can be set equal to the data present at the data inputs (D_o through D_n) by strobing the load (L) input.

Two versions of these IC's are available. Both are four-bit counters. One is configured for binary coded decimal; the other is straight binary. The counters have parallel data (Q_1 through Q_n), borrow (B), and carry (C) outputs which allow them to be cascaded as shown in Figure 9. In the following descriptions of counter applications it will be assumed that the required number of chips has been cascaded and the entire counter will be treated as a single entity.

b. Combined Counter/Adder/Subtracter

A method of using an UP/DOWN counter to combine an addition or subtraction with its counting function is shown in Figure 10. For either case a number, F_1, is first preset into the counter. For the addition case, a frequency, f_2, is then UP counted for one second. At the end of this period the counter contains the sum of F_1 and the measurement, F_2, which would have been obtained if the count had started at zero. For the subtraction case f_2 is applied to the DOWN input for one second and the counter counts down from F_1 to F_1-F_2. If the result is negative it will be in two's complement or binary coded ten's complement form

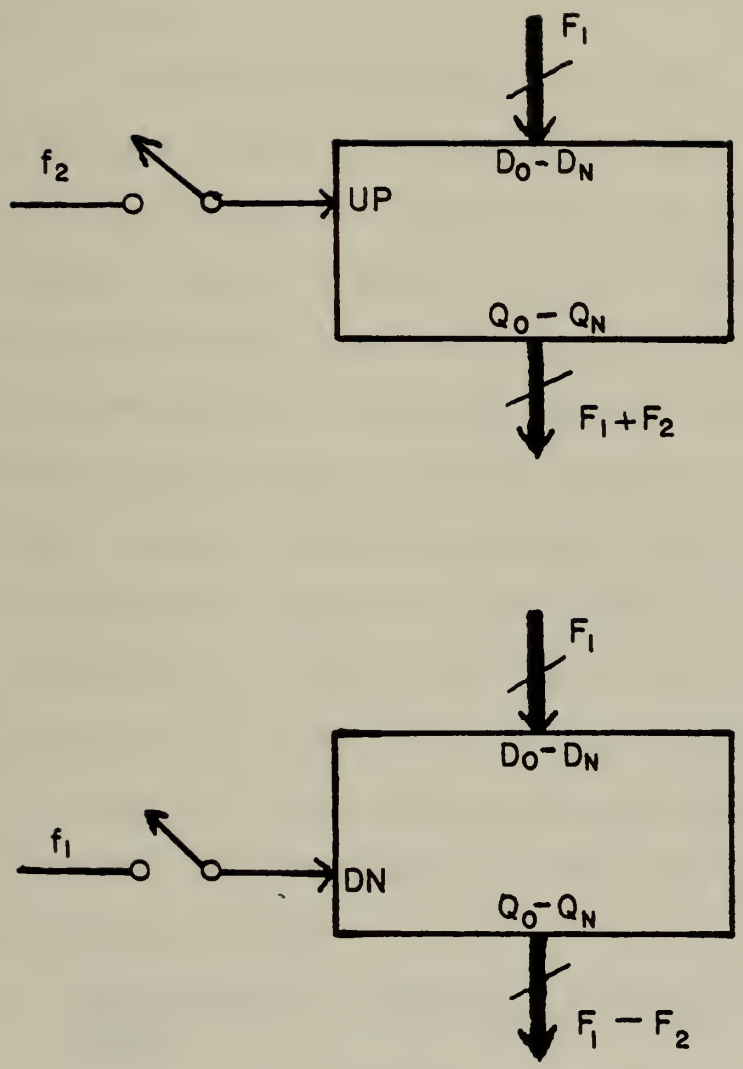


Figure 10 Frequency Computations Using UP/DOWN Counters

depending on the configuration of the counters used. Note that F_1 can be a negative number as long as it is in the correct form.

If the frequencies are stable this method can be extended as shown in Figure 11. Again the number, F_1, is initially loaded into the counter, then the frequencies are counted, one at a time, each for a one-second period. The counts of those counted up add to the result and those counted down subtract from the result. This method can be extended to any number of inputs added and subtracted but it takes a time in seconds equal to the number of frequencies involved to complete a measurement, i.e., four seconds for the counter in Figure 11. This could cause a considerable delay in the effect of a change of one of the frequencies to show up in the output and would similarly reduce the frequency of corrections if this method were used in the AFC system design.

2. Computation Of Operating Frequency And Frequency Error

The method described above for using an UP/DOWN counter to perform additions and subtractions as well as frequency measurement can be applied directly in the AFC system design. To show this, consider the following typical but arbitrary application: The AFC system is to be used with a triple conversion receiver whose operating frequency is defined as $f_o = f_1 - f_2 - f_3 + f_4$. For a given mode

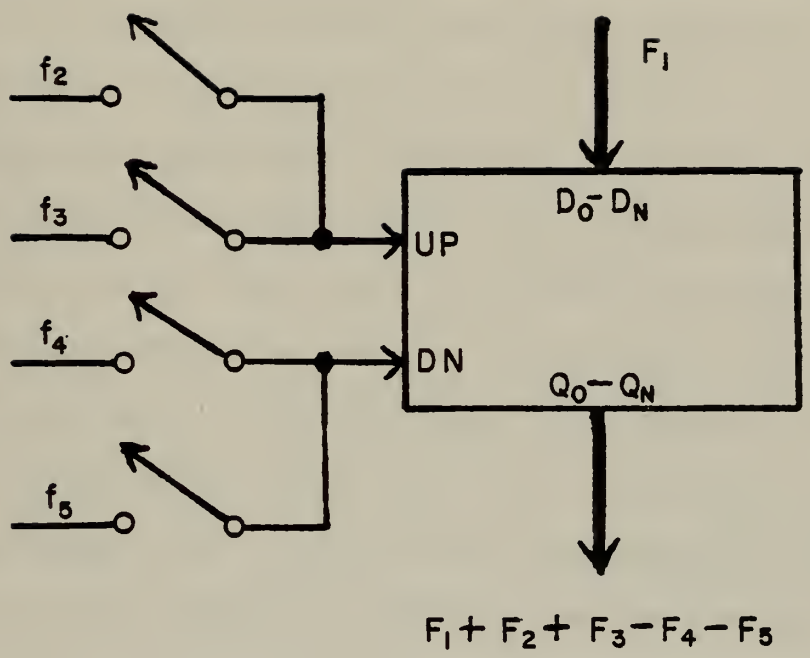


Figure 11 Multi-oscilator Measurement and Computation Using UP/DOWN Counter

and frequency band f_1, f_2, and f_3 are constant. The main tuning oscillator is variable and operates at a frequency f_4.

a. Unlocked Mode

The system diagrammed in Figure 12 is the same as that in Figure 1 except that there is now provision for application to the example multi-oscillator receiver. In the unlocked mode the only purpose of the system is to measure and display the operating frequency. To do this the counter is initially reset to zero. The frequencies are then counted, one at a time, each for exactly one second. Those counted up add to the result. Conversely, those counted down subtract. After the last oscillator is counted the counter contains the number $F_1 - F_2 - F_3 + F_4 = F_o$. This is then loaded into the latch for decoding and display. The counter is then cleared to start a new measurement.

In this example it takes at least four seconds to complete a measurement. This would cause the displayed frequency to lag significantly behind when tuning the receiver from one frequency to another. This would be particularly inconvenient if the receiver had to be set to an exact frequency using only the display as an indicator.

b. Locked Mode

The system diagrammed in Figure 13 is the same as the system in Figure 2 except for the multi-oscillator provision and the use of the counter to perform the error computation. To accomplish this the desired frequency, F_o', is initially loaded into the counter from the latch. The

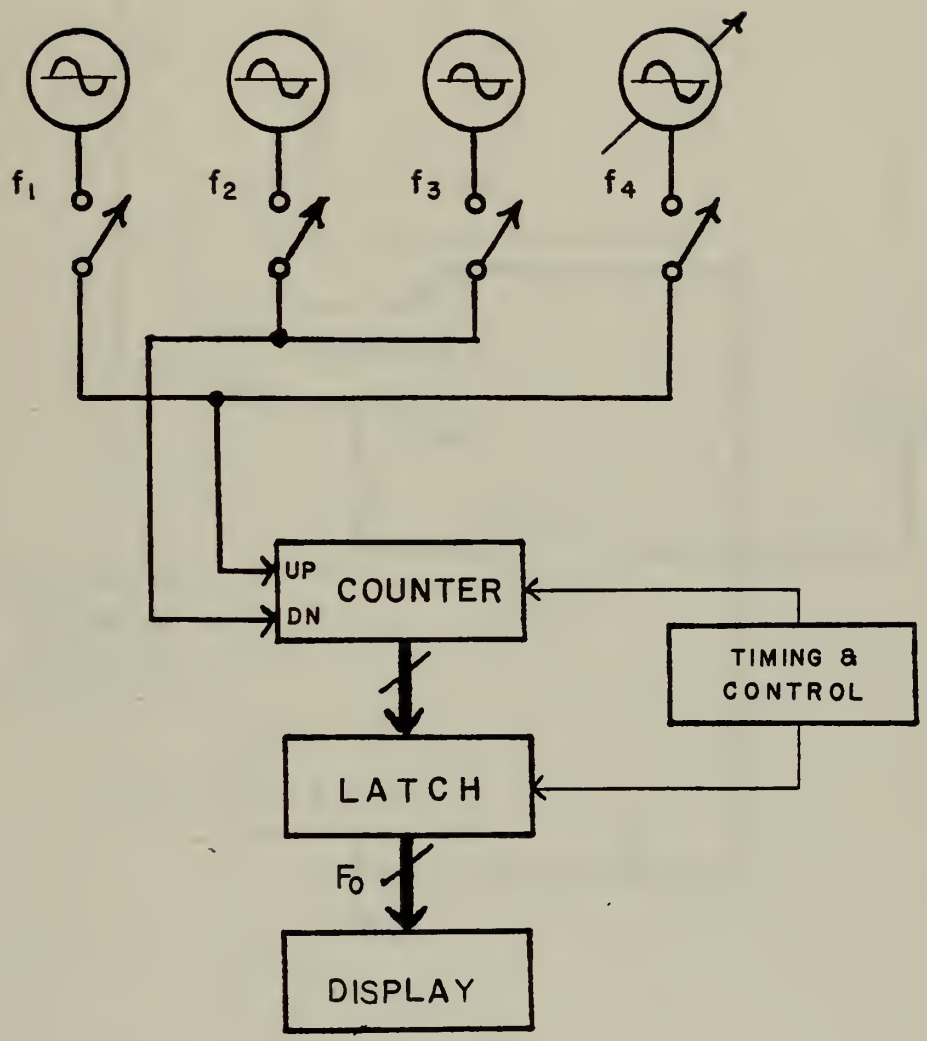


Figure 12 Simplified System -- Unlocked Mode

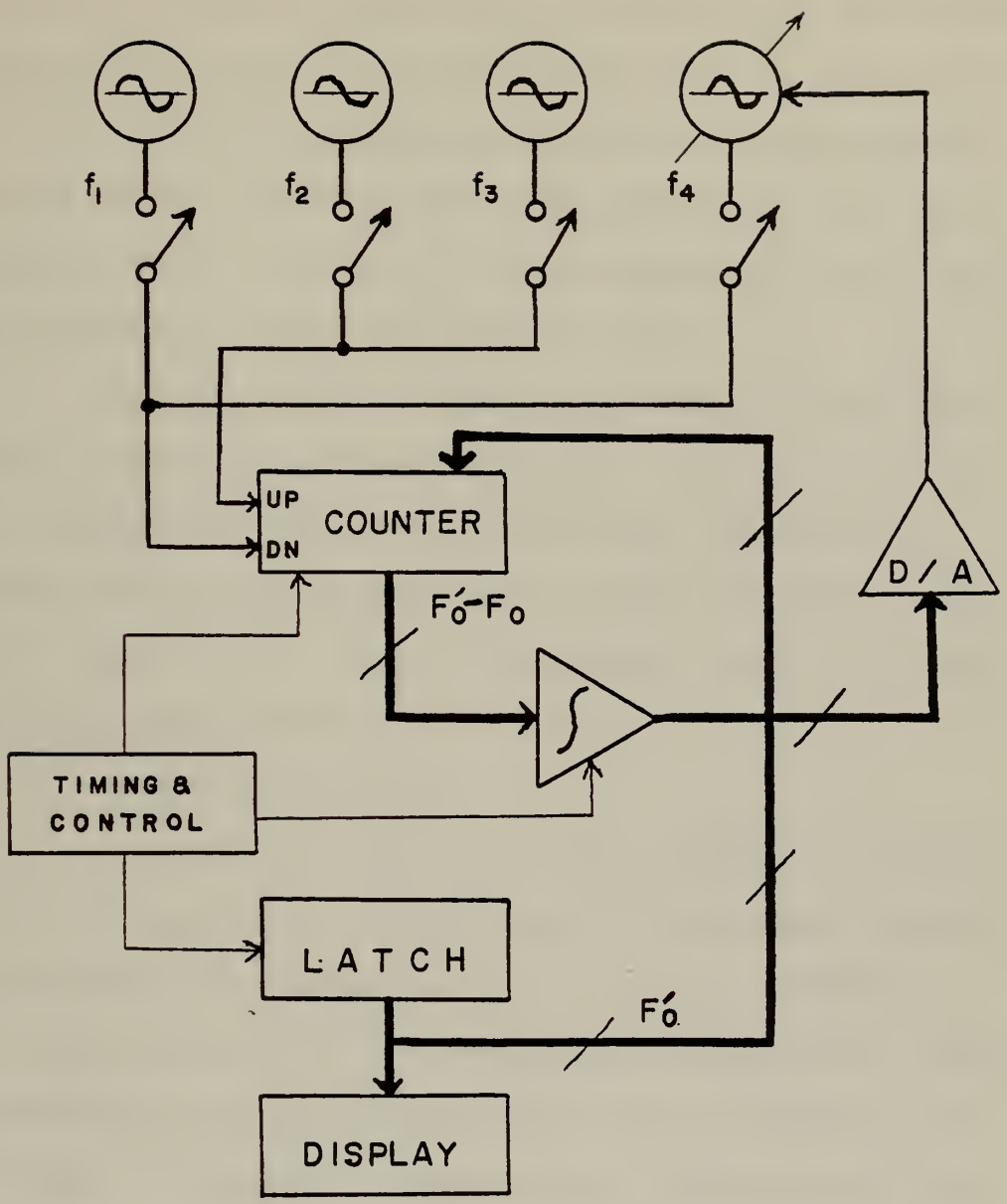


Figure 13 Simplified System -- Locked Mode

frequencies are then counted one at a time as in the unlocked mode except now f_2 and f_3 are counted up and f_1 and f_4 are counted down. At the completion of the four, one-second counts the counter contains the frequency error $F_o' - F_o$. The computed error is input to the integrator, which, with the D/A converter, close the control loop.

Again, in this example it takes at least four seconds to compute the frequency error. As a result the control voltage is updated only once each four seconds. This could significantly slow down a recovery from a step change in frequency or hinder the system's ability to cope with a rapid frequency drift.

c. Design Compromise

A literal translation into hardware of the system shown in Figures 1, 2 and 8 would be extremely complex. The system shown in Figures 12 and 13 is far simpler to realize (only one counter is required to compute the operating frequency or the frequency error) but results in low update rates. A possible compromise is suggested by the characteristics of the equipments with which the system is intended to be used.

A typical HF communications receiver contains a main tuning oscillator and one or more other oscillators. The main tuning oscillator is often the least stable and is the primary reason for needing an AFC system. It is also the oscillator whose frequency is most often changed when the receiver is tuned. The others, which are typically

crystal-controlled and very stable, operate at a fixed frequency for a given mode and band.

A compromise which essentially restores the one-second update rate at a cost of one additional counter and latch is shown in Figures 14 and 15. The primary counter is dedicated to the main tuning oscillator and makes one measurement per second. The secondary counter counts all other oscillators in sequence which, for the example receiver, takes three seconds. The results of the secondary count are stored in the secondary latch for use as data by the primary counter. Otherwise the system is exactly the same as in Figures 12 and 13.

The effects of changes in the main tuning oscillator's frequency are reflected in the display or control voltage once each second. The effects of the other oscillators in this example still take up to four seconds to influence the display or control voltage. Since these oscillators are more stable and their frequencies changed less often this additional delay can be tolerated.

3. Integrator

The primary problem in designing an integrator for the system as so far described is that the frequency error is available only as a parallel number and the D/A converter requires a parallel input. A suitable integrator with parallel input and output could be designed but it would be very complex. An alternative is to select a very simple

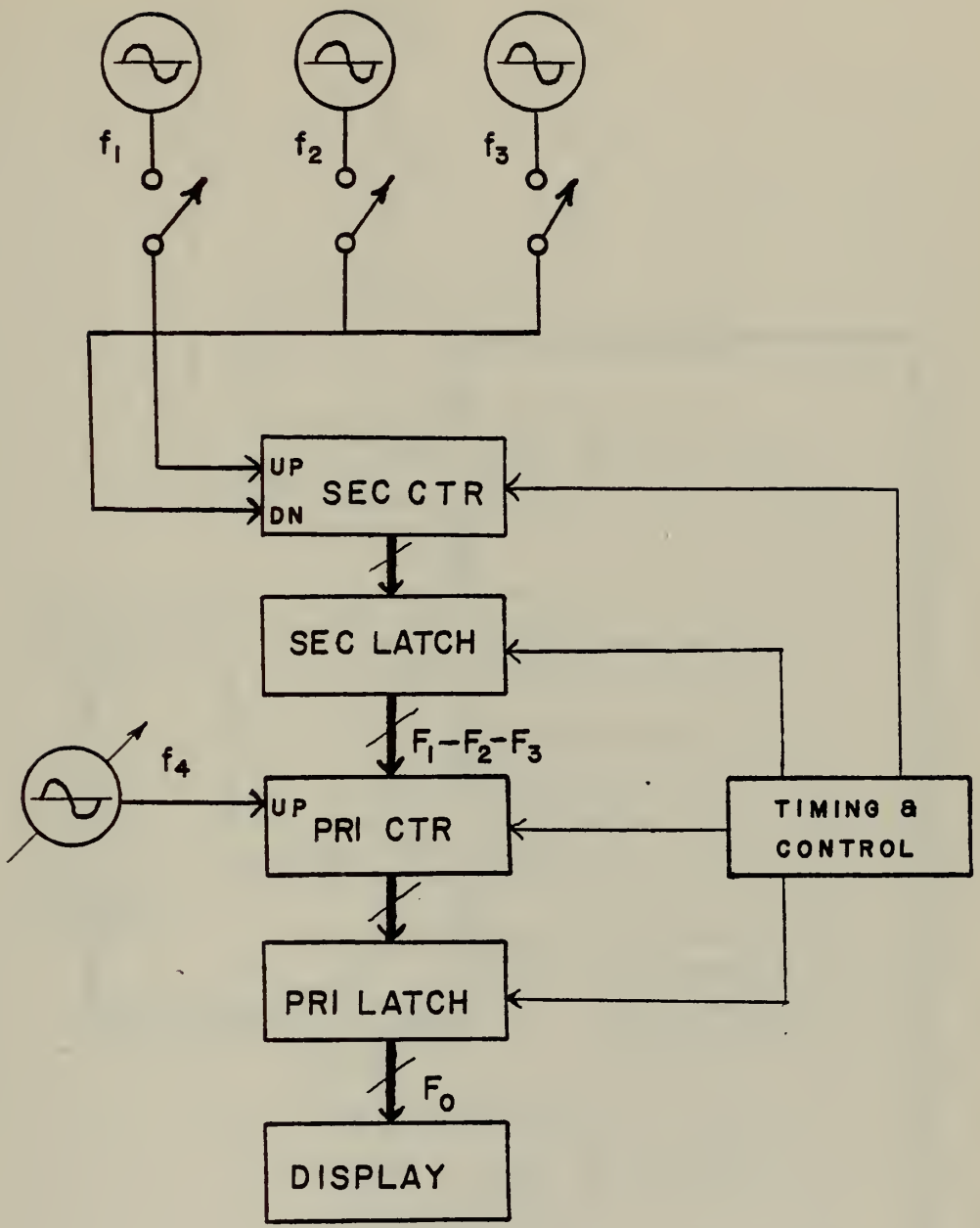


Figure 14 Compromise System -- Unlocked Mode

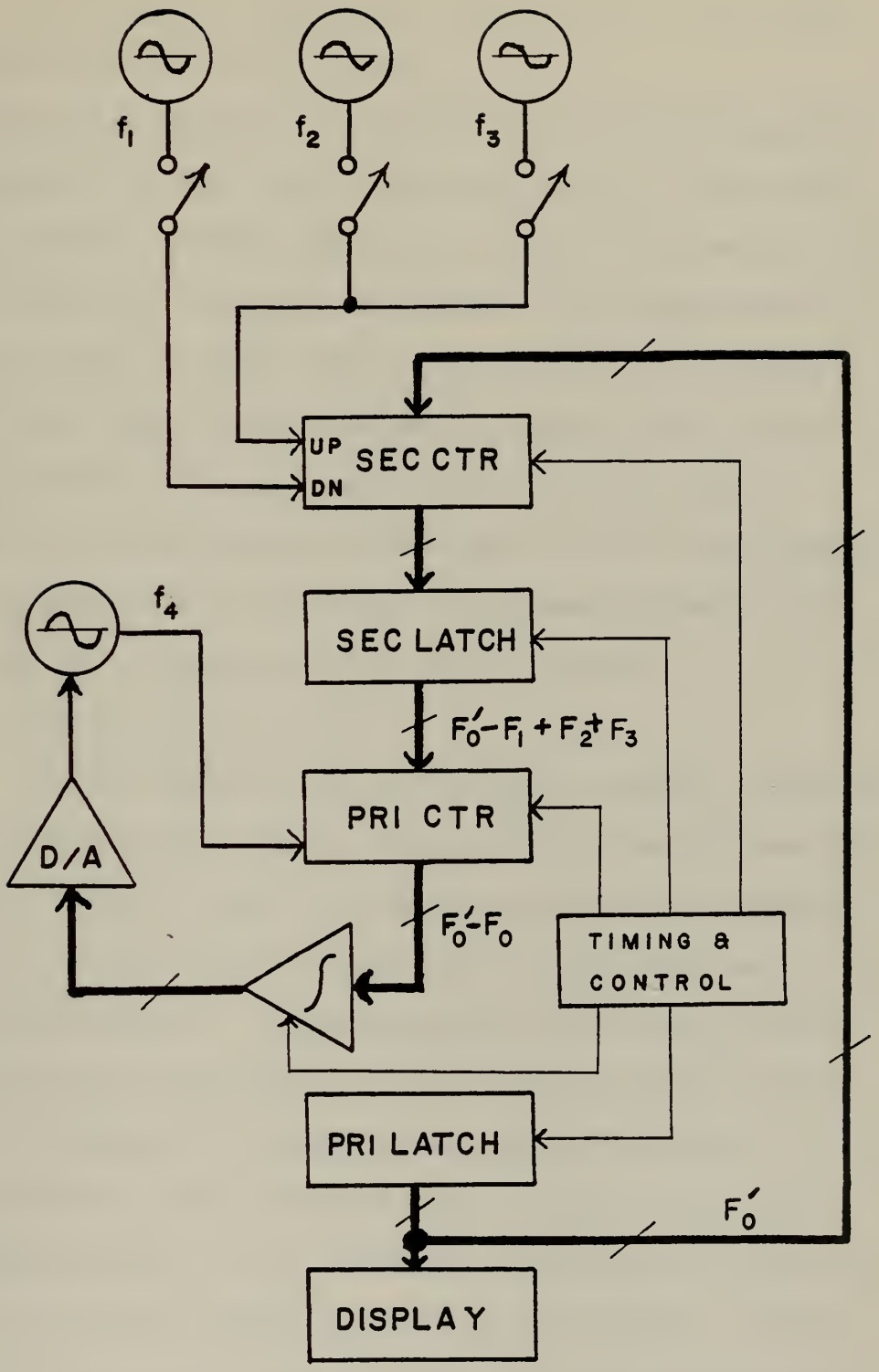


Figure 15 Compromise System -- Locked Mode

integrator circuit and determine if the rest of the system can be easily adapted for its use.

About the simplest integrator possible is the same type of UP/DOWN counter used for computing F_o. The output is in the parallel format required by the D/A converter but the input format is a series of pulses. The magnitude of the input is equal to the number of pulses in the series, the sign of the input is indicated by whether the pulses are applied to the UP input (positive) or DOWN input (negative). In order to take advantage of this very simple integrator the parallel frequency error measurements must be converted to the proper pulse series format.

a. System Modification

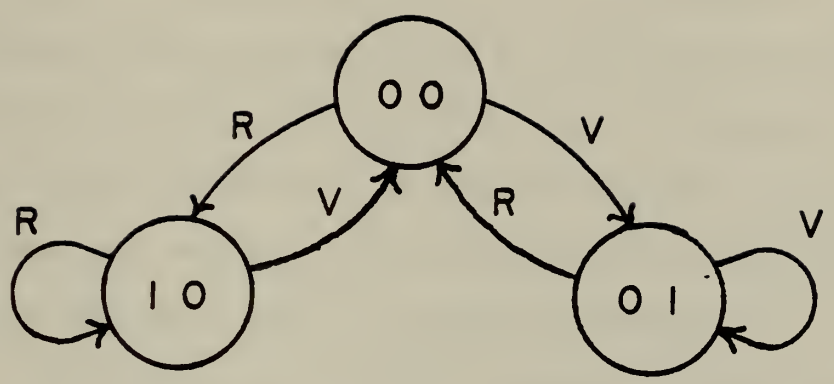
In the locked mode the primary counter contains the error measurement at the end of each one-second measurement period. Another way to view this is that the primary counter is a number of input pulses away from zero equal to the error measurement. A system modification which would provide the error measurement in the required pulse series format is to extend the counting period sufficiently to ensure that zero is always reached and to gate the primary counter input pulses to the integrator during the period between the end of the normal one-second measurement period and the time the counter reaches zero. Depending upon the sign of the error, either of the two events could occur first and initiate the gating of the pulses. Additional circuitry would have to be added to identify which event

occurred first and to route the pulse series to the proper integrator input.

If the primary counter's counting period were not extended in the locked mode the count would never reach zero for operating frequencies less than the desired frequency. The amount of the extension could be determined by testing for the occurrence of both the end of the normal one-second measurement period and the counter reaching zero. Alternately, the counting period could be extended by a fixed amount large enough to ensure the count reaching zero for the worst case error the system is intended to cope with. The latter choice was used in the design because it was simpler to implement.

Circuitry for gating the pulses to the integrator would require signals marking the delimiting events. A signal marking the end of the normal one-second timing interval can be generated by the timing and control logic. A signal marking the zero crossing of the count in the primary counter is already available as the "borrow" and "carry" outputs. When the counter is counting up it produces a "carry" output as it overflows through zero. When it is counting down, as in the system of Figure 15, a "borrow" is output as it underflows through zero.

Figure 16 is a transition diagram of the required steering logic. The states are the outputs of the circuit, U and D. The transitions are to be caused by the leading edge of the input signals, R and V. The outputs



States = Outputs (UD)

UD = 11 Is Forbiden

Figure 16 Steering Logic State Transition Diagram

are normally at state 00. If an R input arrives first the output goes to state 10 and remains in that state, regardless of further R inputs, until a V input arrives. At that time the output returns to state 00. Alternately, if the V input arrives first the output goes to state 01 until an R input arrives. An output state of 11 is forbidden. A circuit to realize these requirements would be moderately complex at the gate level, but not difficult to design. An integrated circuit designed for phase detector applications and which has the required state transition characteristics is available and was used in the actual design.

Figure 17 is a partial diagram of the system of Figure 15 modified to use the simple UP/DOWN counter integrator. When the operating frequency is less than the desired frequency the normal one-second measurement period ends before the count reaches zero, causing the steering logic's U output to go high and pulses to be gated to the integrator's UP input. When the count reaches zero a number of pulses equal to the magnitude of the error would have been gated to the integrator. The borrow output from the primary counter causes the steering logic's U output to go low, terminating the pulse string to the integrator. When the operating frequency is higher than the desired frequency the system acts in a similar manner except the count reaches zero before the end of one second and pulses are gated to the integrator's DN input from then until the end of the normal one-second measurement period.

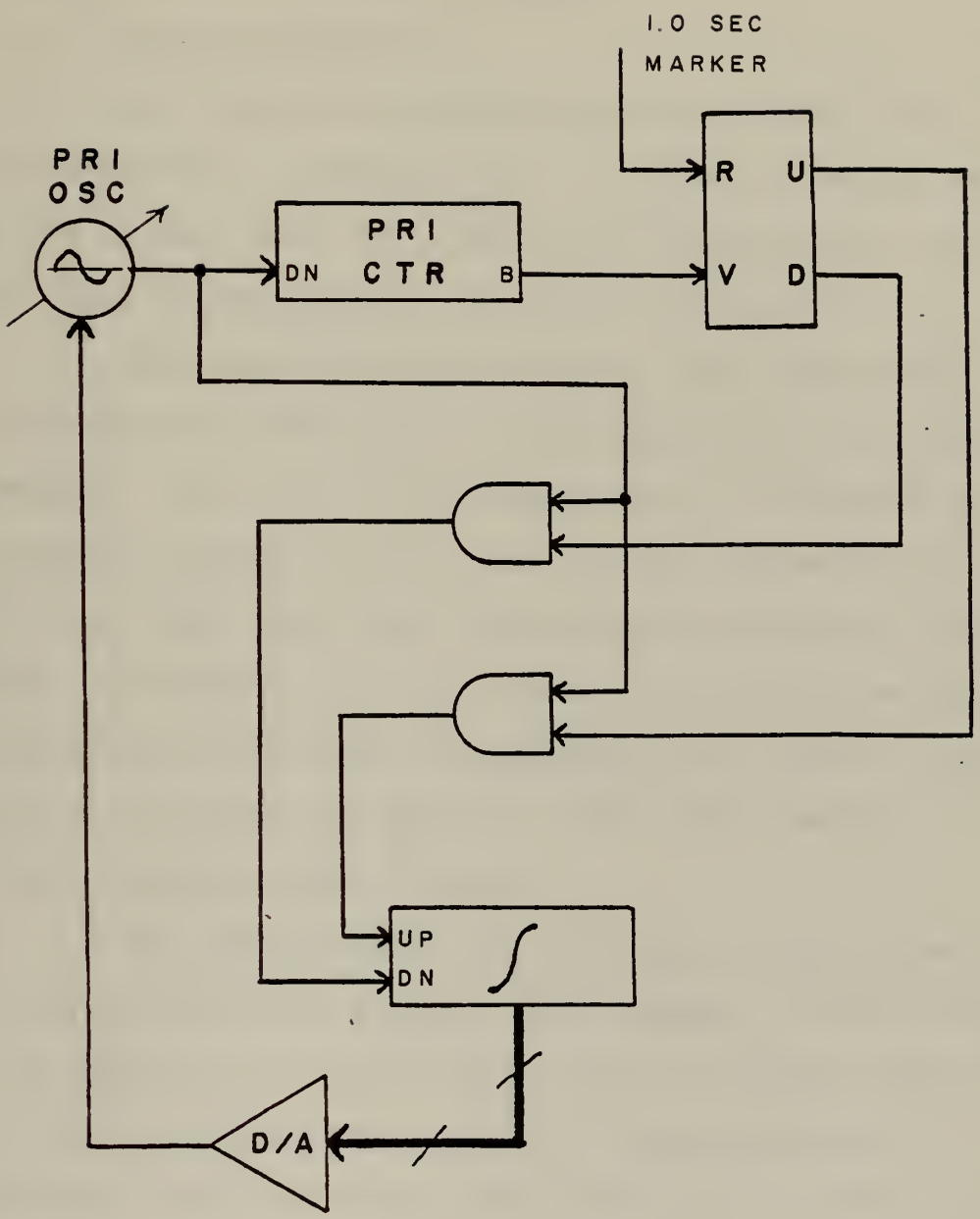


Figure 17 System Modification for Simple Digital Integrator

The approach shown in Figure 17 is essentially that used in the final system design.

b. Analog Integrator

In a sense the steering logic provides the error measurement in analog form. By using an analog integrator the design would not require an expensive D/A converter. Such an arrangement is shown in Figure 18.

The outputs of the steering logic are pulses whose widths are proportional to the magnitude of the error measurement. The sign of the measurement is indicated by which output the pulse comes from. If the pulses are of constant and equal amplitude then the time average of the algebraic difference wave form U-D is an accurate analog representation of the error measurement and could be input directly to an analog integrator. This could result in a significant system simplification.

The problem with this approach is the extremely small duty cycle of the pulses. For example, if the oscillator in Figure 18 is operating at about 5 MHz and there is a 2 Hz error the pulse width would be approximately 0.4 microsecond. The integrator would have to be capable of accurately processing this short pulse, then maintain a constant output for the one-second interval until the end of the next measurement. Any drift in the integrator output would induce frequency drift in the oscillator. An adequate integrator would have to have exceptional band width and stability. Circuits to meet these requirements would be

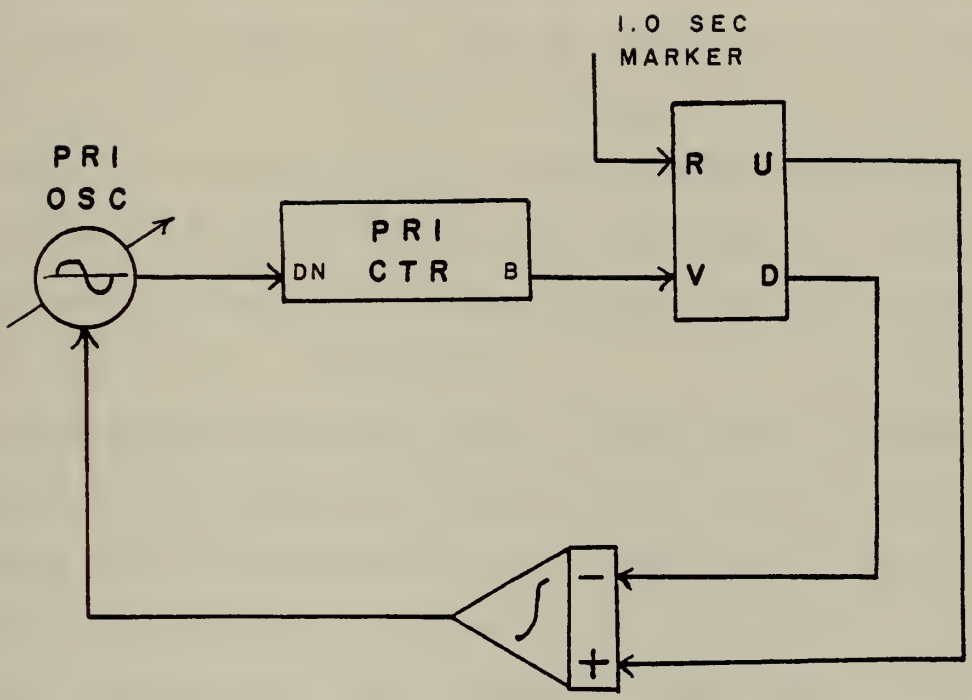


Figure 18 System Modification for Analog Integrator

expensive and would require precise adjustment. For these reasons no attempt was made to use an analog integrator.

4. Timing And Control

The AFC system design selected for implementation is that shown in Figure 19. This is the same as that shown in Figures 14 and 15 as modified by Figure 17. In order for this system to operate properly, very accurate timing signals must be provided to delimit the measurement intervals and sequence the transfer of data between the various portions of the system. Additionally, control must be maintained over signal and data paths to configure the system properly for the desired mode and provide for an orderly transition from the unlocked to the locked mode. Provision also had to be made for programming the system for the hetrodyne scheme used by the equipment being controlled.

Once the specific timing and control requirements were established, the design of circuitry to meet these requirements was straightforward and presented no particular problems. This circuitry is described in detail in a subsequent section. The state descriptions which follow do not uniquely satisfy the requirements because the relative sequence of some operations is unimportant. They do describe the sequencing of states in the final system design.

In the following descriptions, "primary oscillator" refers to the variable frequency oscillator whose frequency is measured by the primary counter; "secondary oscillators" refers to all other oscillators in the hetrodyne scheme

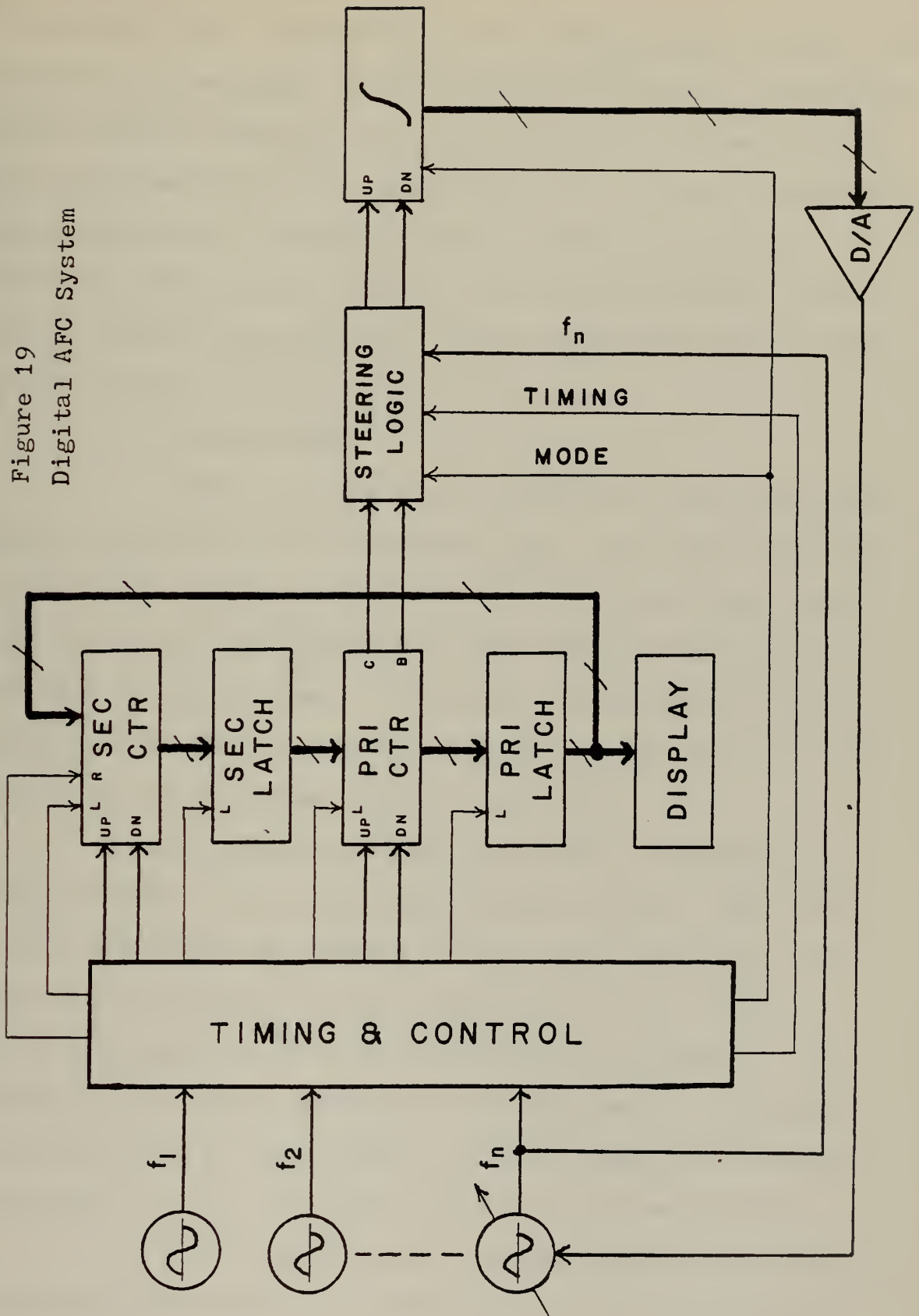


Figure 19
Digital AFC System

being used. The frequencies of the secondary oscillators are measured, in sequence, by the secondary counter. "Secondary update cycle" refers to the time between the times valid data is entered into the secondary latch. This is equal to approximately N-1 seconds for an N oscillator scheme. "Primary update cycle" refers to the (approximately) one-second interval from the end of one measurement made by the primary counter until the end of the next.

a. Unlocked Mode

Figure 20 is a state diagram for the timing and control circuitry in the unlocked mode. The only function of the system in the unlocked mode is to measure and display the operating frequency of the communications device to which it is attached. Therefore, the operation of the integrator is inhibited and its output is forced to be null (midrange) at all times while in this mode.

No special provision was made for entering the unlocked mode in any particular control state. This could as much as double the amount of time until the first valid frequency is displayed (about eight seconds instead of about four seconds for a four-oscillator equipment). This should not cause any particular inconvenience in operating the system and the additional circuitry required to force a particular initial state was not felt to be warranted.

There are two paths through the control states; the system traverses one or the other of these paths once each primary update cycle. Which path is used is determined

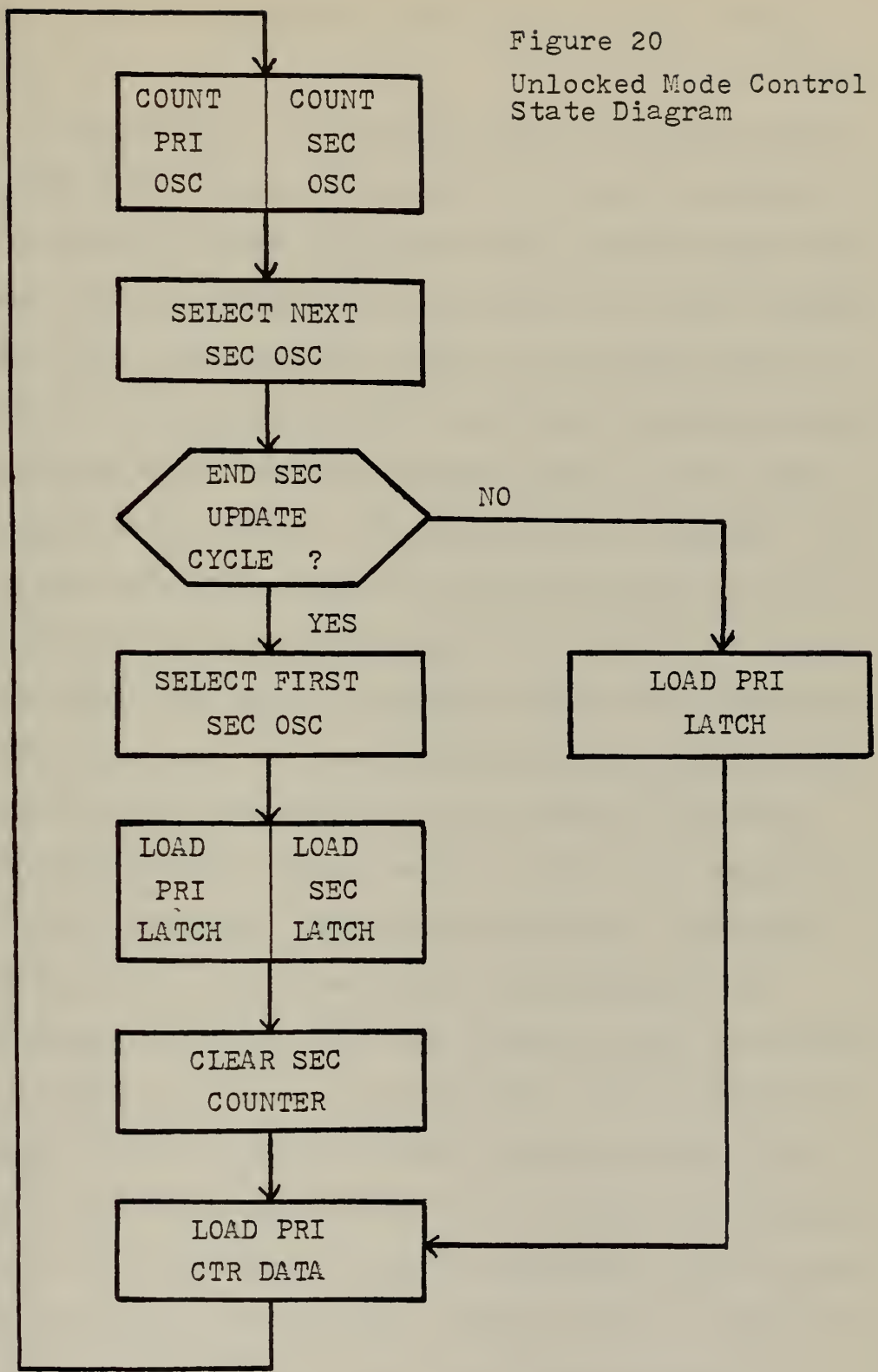


Figure 20

Unlocked Mode Control State Diagram

by whether or not a secondary update cycle is also being completed.

Assume that a secondary update cycle has just begun and the first count of the cycle is about to begin. The control state is that depicted at the top of Figure 20. The primary counter contains the results of the last secondary update cycle; the secondary counter has been reset to zero. The primary oscillator and the first secondary oscillator are connected to the appropriate input of the appropriate counter and a precise one-second count is made. At the end of the count the primary counter contains the current operating frequency measurement, F_o, and the secondary counter contains + or $-F_1$ as appropriate for the hetrodyne scheme. Then the next secondary oscillator is selected in preparation for the next count and the control circuitry detects whether or not this exceeds the number of oscillators for which the system has been programmed. Assuming that there are two or more secondary oscillators, the secondary update cycle has not been completed and the states follow the right hand path of the diagram. The contents of the primary counter, F_o, are loaded into the primary latch replacing the previous measurement for decoding and display. The results of the previous complete secondary update cycle are again loaded into the primary counter and the system is again in the control state at the top of the diagram. Another set of counts is made. The secondary counter now contains $\pm F_1 \pm F_2$ and the primary counter again contains F_o.

The same loop is followed until the last secondary oscillator has been counted. At that time the control circuitry detects an attempt to select an oscillator for which the system has not been programmed, indicating the end of a secondary update cycle. The secondary counter now contains a complete secondary frequency measurement and the control state sequence follows the left hand path on the diagram. The first secondary counter is selected in preparation for the next measurement. Then the current valid measurements are loaded into both the primary and secondary latches and the system is prepared for the next measurement by clearing the secondary counter and loading the new secondary measurement into the primary counter. The system is now in the same control state as it was at the beginning of this description. This sequence is repeated as long as the system is in the unlocked mode.

b. Locked Mode

Control of the system in the locked mode is slightly more complicated than in the unlocked mode but remains basically the same. The first difference is that the locked mode is entered by forcing a known state in order to minimize the time until the first frequency correction is made. Secondly, the integrator is disabled in the unlocked mode and it remains disabled in the locked mode until the end of the first secondary update cycle. This prevents erroneous "corrections" from being made until the first valid locked mode measurement has been completed. A third difference is that at the beginning of a secondary

update cycle the desired frequency is loaded into the secondary counter from the primary latch. The "clear secondary counter" state is retained but it is a "do-nothing" state in the locked mode so there was no reason to add circuitry to disable it. A fourth difference is that the primary counter no longer makes precise one-second counts but makes error measurements as previously described. Finally, the direction of all counts (up or down) is reversed and the contents of the primary latch never change. The control states are shown in Figure 21.

5. System Dynamics

The basic concept for this AFC system was patterned after the phase locked loop but continuous, linear control theory, usually used for modeling phase locked loops, is not appropriate for the analysis of this system. It can be more accurately modeled as a discrete network.

The simple, first order discrete network shown in Figure 22 parallels the actual system configuration very closely and can be used to accurately predict system performance. In this model the operating frequency has been normalized to zero. The input, D(z), is the uncorrected frequency error. The output, E(z), is the frequency error after correction. The gain, k, is the overall loop gain and is equal to the magnitude of the correction resulting from the detection of a unit error. More specifically, k is equal to the product of the error-to-voltage gain of the

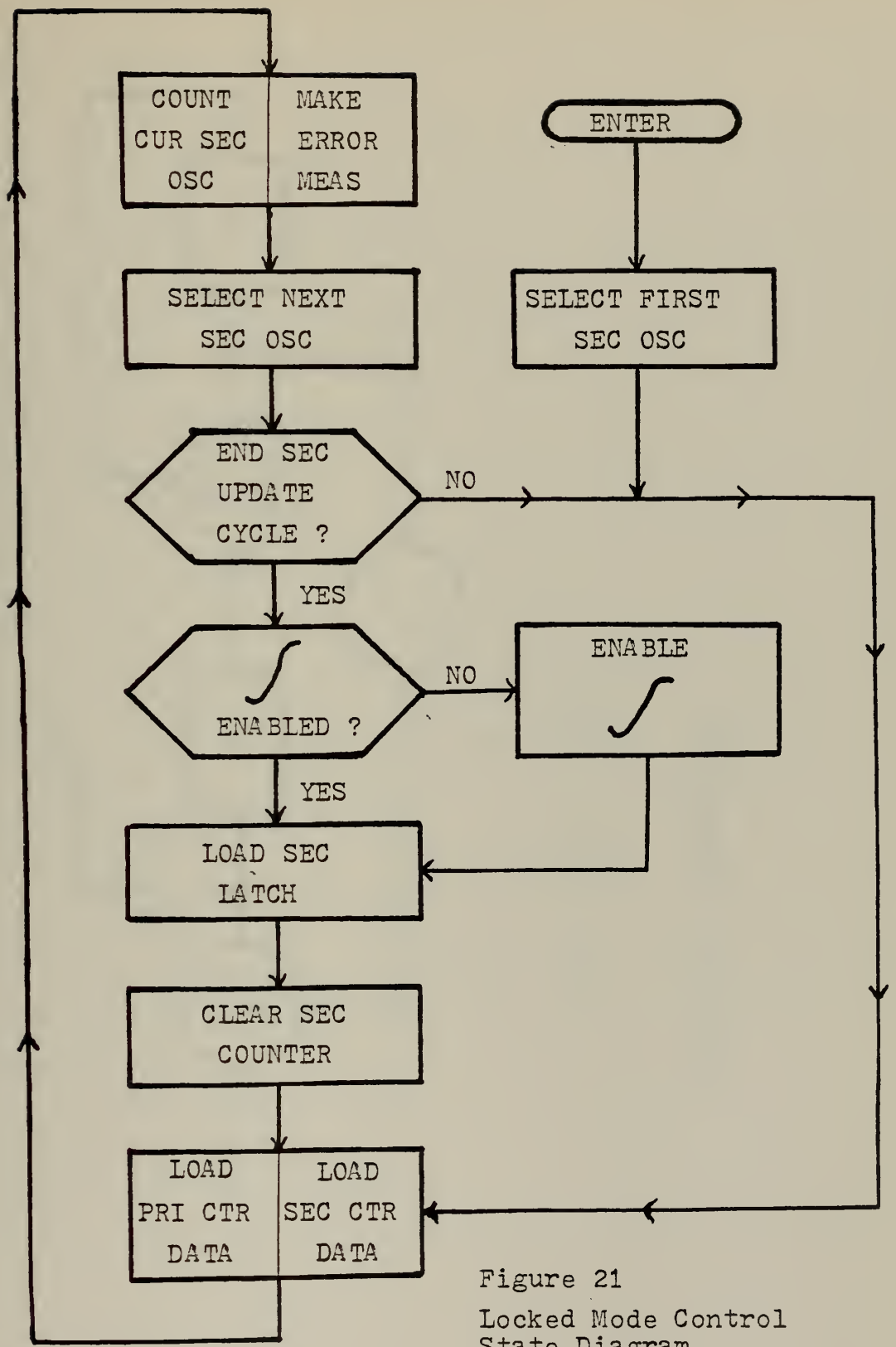
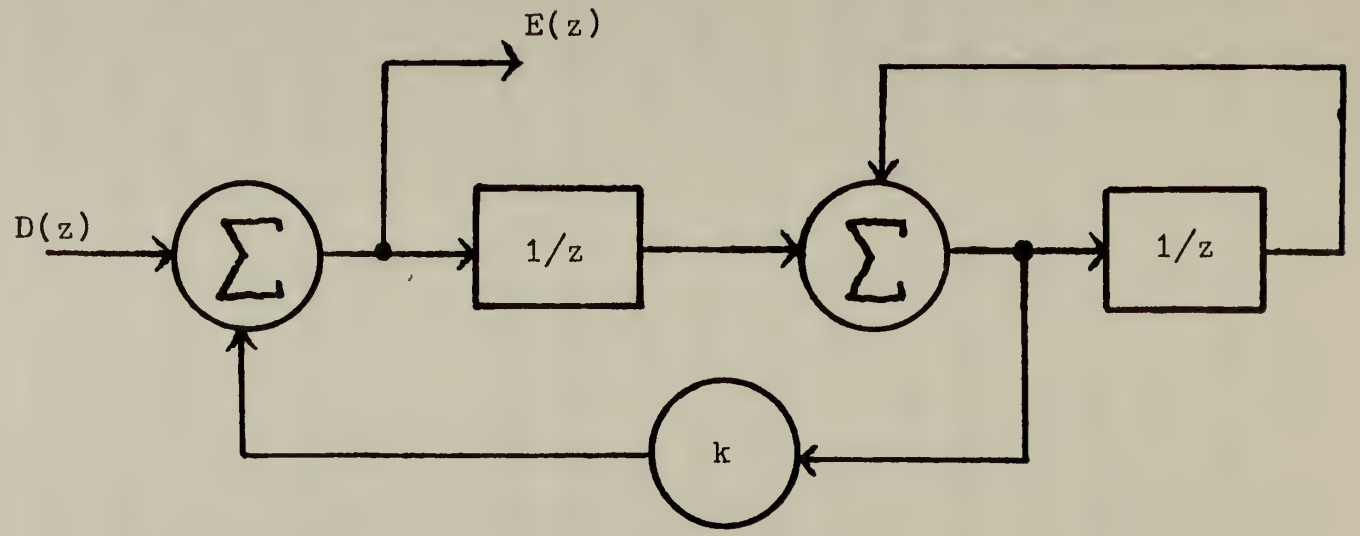


Figure 21

Locked Mode Control
State Diagram



$$H(z) = \frac{E(z)}{D(z)} = \frac{z-1}{z-(1-k)}$$

Figure 22 System Model

AFC system and the voltage-to-frequency gain of the modified primary oscillator.

As with most models, this one contains simplifications. The first is that the voltage-to-frequency gain function of the primary oscillator is not linear and can be a function of both the operating frequency and the magnitude of the control voltage. By careful design of the VCO modification the non-linearity can be minimized and for moderate changes in the error correction voltage a linear approximation is adequate. The second simplification is that in this system the error measurement is actually a measurement of the average error over a one-second measurement interval. To include this explicitly in the model would increase its complexity unnecessarily. This factor can be included in specifying D(z) and interpreting the resulting E(z).

A factor which is not a limitation of the model but which must be included in interpreting the results obtained is the effects of quantization. This is no less true for discrete networks in general.

The loop gain, k, is the only parameter available for establishing any desired characteristics in the system dynamics. The first step in selecting a value for k is to decide what the desired characteristics are and what are their relative importances.

The motivation for designing this system was to correct for drifts in the operating frequency. While the rate

of uncorrected drift would vary as a function of time, for short intervals it can be modeled by making D(z) correspond to a ramp function. In this case it is desirable to minimize both the peak and average corrected frequency error.

Another possible type of frequency error is a step change in frequency caused by some mechanical or electrical shock to the communications equipment. This can be modeled by making D(z) correspond to a step function. In this case it is desirable to recover to the operating frequency in as short a time as possible.

The remaining factor to be considered is the interaction of system dynamics and quantization effects. It is desirable to minimize these effects.

a. Step Response

While not a highly likely occurrence, a sudden shift in the operating frequency of the controlled equipment is possible and the AFC system must be able to properly correct the associated step frequency error. This case is treated first because it is simpler. If the uncorrected error is a step function with amplitude A, then:

$$D(z) = \frac{Az}{z-1}$$

and:

$$E(z) = D(z)H(z) = \frac{Az}{z-1} \quad \frac{z-1}{z-(1-k)} = \frac{Az}{z-(1-k)}$$

Taking the inverse transform:

$$e(nT) = A\ (1-k)^n$$

where T is the period between error measurements and n is the number of the current measurement period.

From this we can conclude that e(nT) will converge to zero for $0<k<2$. The rate of convergence is a function of $|1-k|$, e.g., the rate of convergence is the same for $k = 0.5$ and $k = 1.5$. The highest rates of convergence are for values of k in the neighborhood of one, the lowest rates in the neighborhoods of zero and two.

b. Drift Response

A more general situation is when, at a given point of time, there exists an instantaneous error of magnitude A and the operating frequency is drifting at a rate B. In this case the uncorrected error is the sum of a constant and a ramp function, and

$$D(z) = \frac{Az}{z-1} + \frac{BTz}{(z-1)^2}$$

Then:

$$E(z) = D(z)H(z) = \frac{Az}{z-(1-k)} + \frac{BTz}{(z-1)[z-(1-k)]}$$

Taking the inverse transform:

$$e(nT) = A(1-k)^n + \frac{BT}{k}\ [1-(1-k)^n]$$

The transient terms will decay, depending upon the value of k, in the same manner as the step response. Interpreting the steady state term, BT/k, is more difficult.

The steady state term is actually the average steady state error because of the averaging effect in the measurement method used. Since the uncorrected error is changing at a constant rate, B, and corrections are made every T seconds, the maximum error (after the transients decay) is: $(BT/k) + (BT/2)$ or $(BT/k) - (BT/2)$ whichever has the larger magnitude.

From this it can be concluded that both the average and peak errors are reduced for larger values of k. The value must still be in the range $0<k<2$ to provide correct transient performance.

c. Quantization Effects

The primary and secondary counters and the integrator represent calculations and measurements in binary or binary-coded decimal format. These numerical representations can only take on integer values and, due to the finite capacity of the hardware, only over a finite range. Additionally, the quantization of measurements to integer values is not a simple truncation or rounding. Due to the pseudo-random relationship of the phase of the measurement period and the phase of the signal being counted, the "rounding" can go in either direction. This effect is often noticeable in laboratory frequency counters as "last digit jitter."

If the communications equipment being controlled has N oscillators in its hetrodyne scheme, the "jitter" in the computed frequency would be over a range N. This is over and above changes due to actual variations in operating

frequency. These variations will also appear in the error measurement and the effect of such random variations on system operation must be considered.

The expected value of the measurement is the value measured. In the case of the error measurements, the integrator will tend to average out the variations if, over the short term, the variations do not produce unstable responses in the control loop. The effects of these variations and quantization effects in general can be minimized by selecting a value for k near zero.

d. Selecting Loop Gain

The "quality" of a communications device would probably be constant throughout its design. For example, if a particular radio receiver has good short-term frequency stability it is probable that it would also have good mechanical stability. On the other hand, a "poor quality" radio receiver would likely be deficient in both its electrical and mechanical characteristics.

It has been observed that system stability requires that the loop gain be in the range $0<k<2$ and that transient response is a function of $|1-k|$. It was further observed that transients decay most rapidly for loop gains in the neighborhood of one, steady state errors for drift correction are minimized for loop gains in the neighborhood of two and quantization effects are minimized for loop gains in the neighborhood of zero.

If the system is used with a "poor quality" communications device, it must be able to cope with relatively high drift rates and be able to recover rapidly from step changes in frequency. Quantization effects are of little importance because the induced variations in frequency would be masked by the existing short-term instability of the equipment. In this case a loop gain somewhat greater than one would be appropriate. The nearness to one would give good transient recovery and being greater than one reduces the steady state drift error.

The system was designed to operate with a "good quality" communications device. In this case the probability of a step change in frequency is low and the importance of transients is similarly reduced. The good short-term stability would allow the use of low values of loop gain without exceeding reasonable limits on steady state drift error. This would in turn allow the minimization of quantization effects. In general, the better the short-term stability the lower a value of k should be used. Values in the range $0.25<k<0.5$ would retain adequate transient recovery and drift performance while minimizing quantization effects.

III. DESIGN DETAILS

The hardware implementation of the design shown in Figure 19 was straightforward. Except for the timing and control circuitry, completing the design consisted of simply selecting the appropriate counter, latch and decoder devices and cascading them in appropriate numbers to handle the expected measurement magnitudes. The timing and control circuitry is less repetitive. Even though it accounts for only a modest fraction of the total system circuitry, and its function is ancillary to the overall design, it does represent a very significant portion of the design effort and will be described in detail in this section.

A. COUNTERS, LATCHES AND DECODER

The communications equipments for which this AFC system was designed operate at a maximum frequency of about 30 MHz. Since the system was designed to measure and display the frequency to the nearest Hertz, a total capacity of eight decimal digits is required. Therefore, each of the counters and latches and the decoder are eight decimal digits wide. Since these sections were implemented with integrated circuits having a capacity of one binary-coded decimal digit, each section consists of eight cascaded integrated circuits.

B. TIME BASE

Figure 23 is a diagram of the system's time base and Figure 24 is a diagram of its output waveforms. In most respects it is similar to the timebase for a conventional frequency counter but some additional complexity was required for generating signals to properly sequence the transition from the unlocked to the locked mode.

All of the timing waveforms are derived from the accurate and stable output of a crystal-controlled 4 MHz oscillator. The 4 MHz signal is divided down to 100 Hertz by U1 through U5, and except for the deviations described below, it is further divided down to 10, 1.0 and 0.5 Hertz by U6, U7 and U8A respectively.

The precise 1.0-second timing period corresponds to the low half period of the output of U8A. Any phase jitter caused by variations in propagation delay and ripple carries is removed by U8B.

At the end of one second the output of U8A goes high and the contents of U6 and U7 are both zero. The high output of U8A causes the outputs of U8B to change state and U9 to gate the contents of U6 to U10 where they are decoded. The unused "zero" output, $\overline{P0}$, of U10 immediately goes low. Ten milliseconds later the contents of U6 advance to one, the "zero" output of U10 goes high and the "one" output, $\overline{P1}$, goes low. Each ten milliseconds the contents of U6 are advanced and corresponding low-going pulses are output from the decode outputs of U10. When U6 advances to eight, the

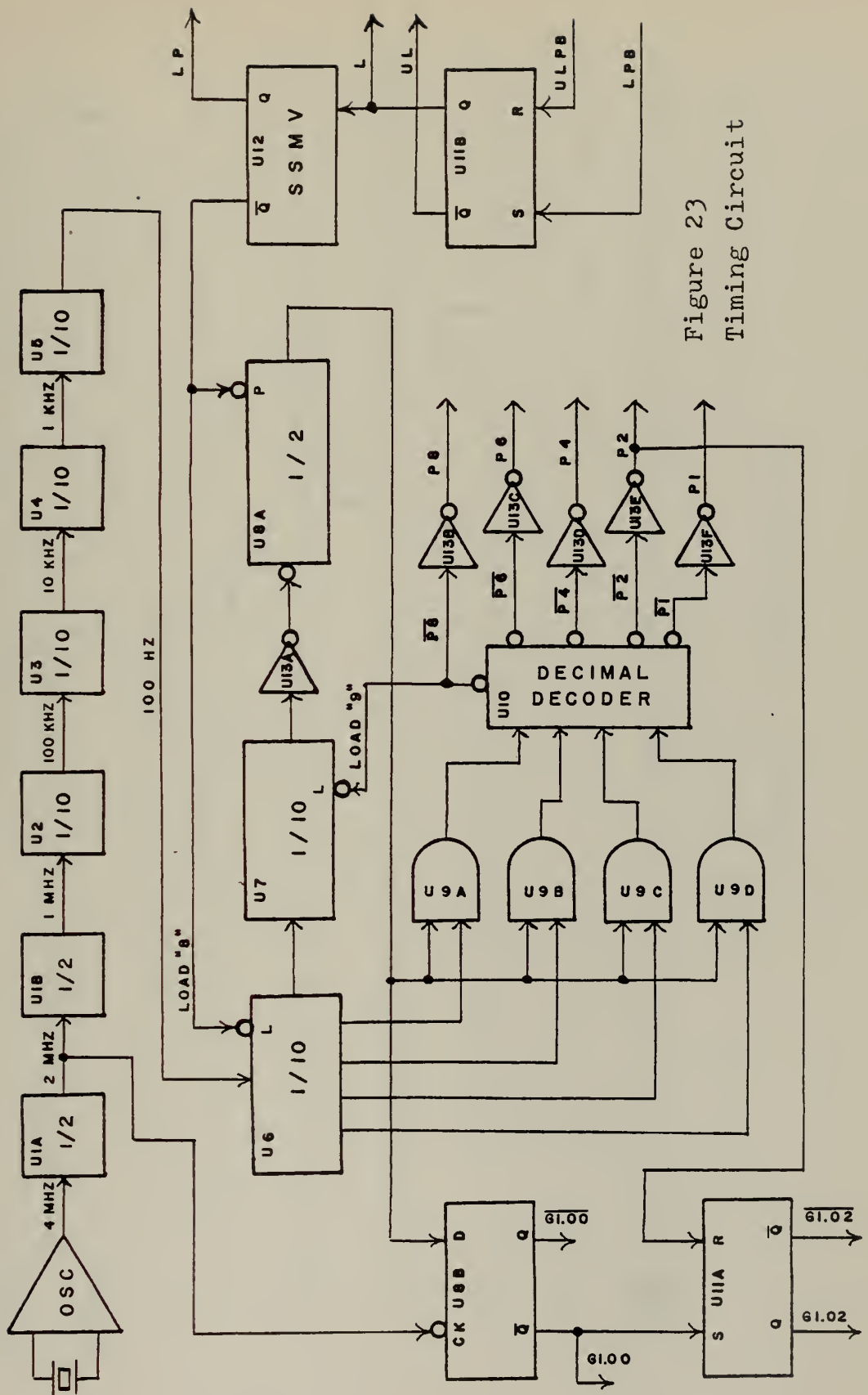


Figure 23
Timing Circuit

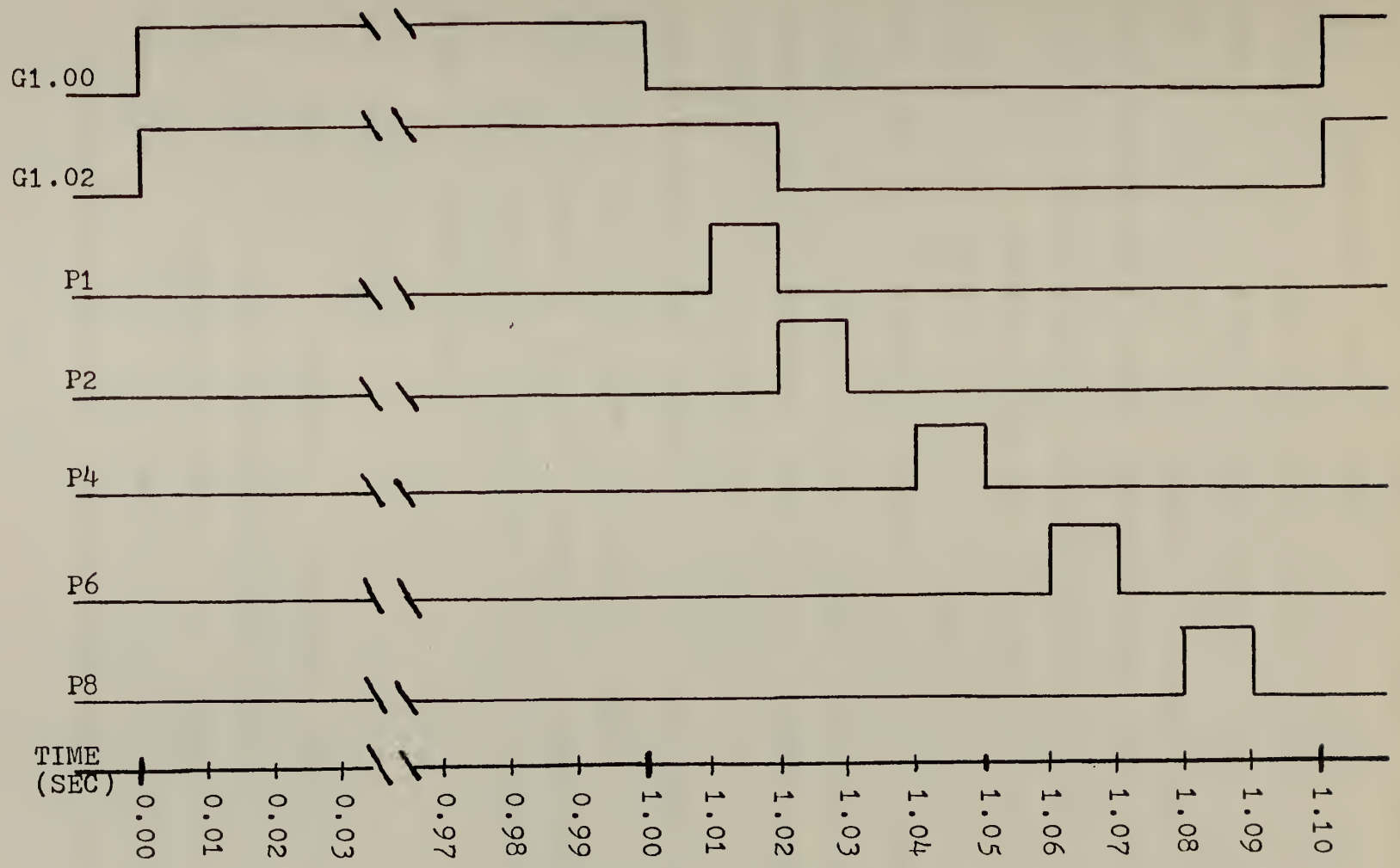


Figure 24 Timing Diagram

"eight" output, $\overline{P8}$, of U10 goes low causing the contents of U7 to change from zero to nine. This causes a ten-to-one speedup of the high half-period of the output of U8A, shortening it to 0.1 second. This further results in limiting U6 to producing only one sequence of outputs from U10. U13B through U13F invert selected outputs from U10 to produce high-going pulses for sequencing the control logic.

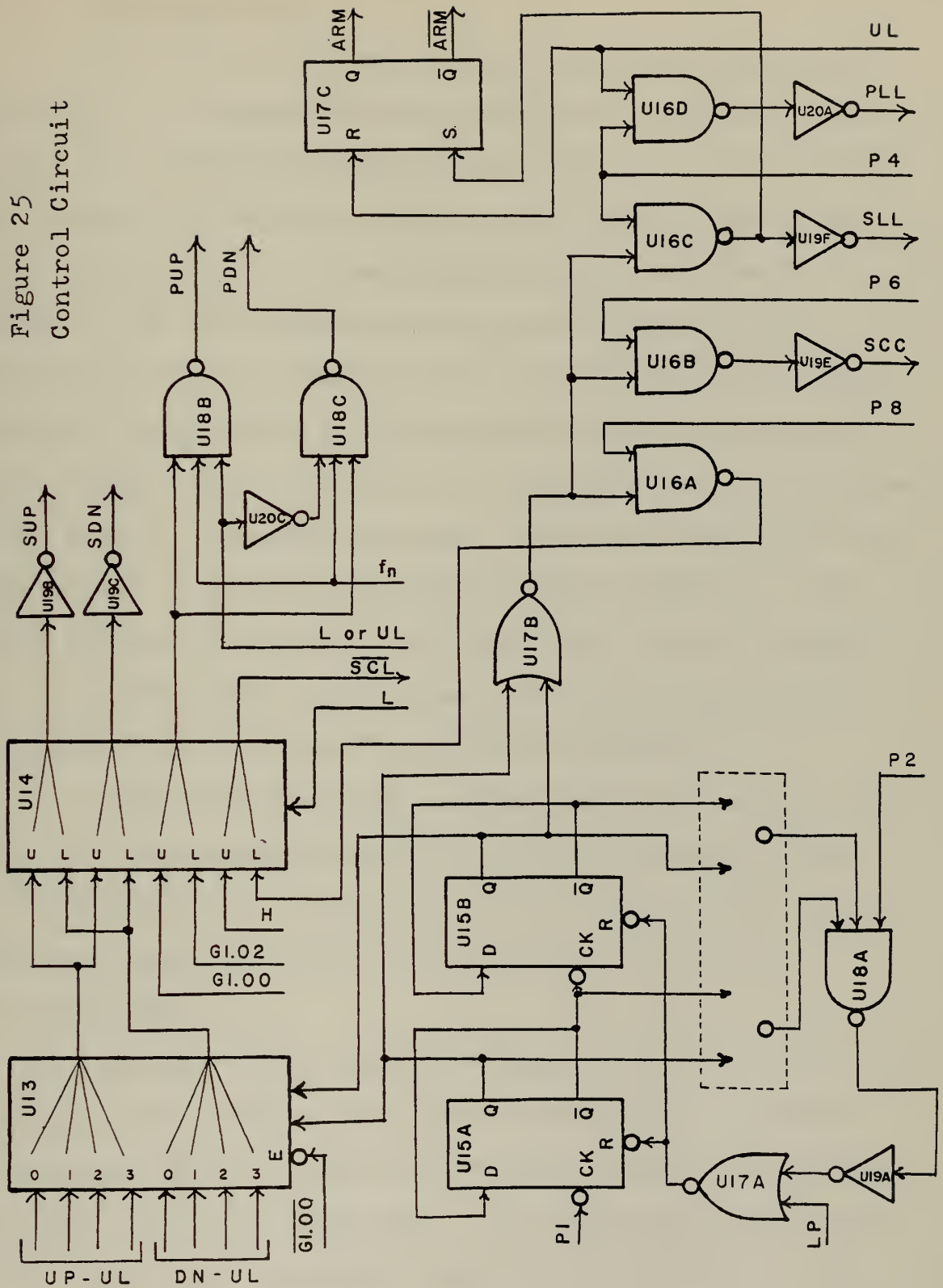
U11B is the mode latch and its state is controlled by front panel "lock" and "unlock" pushbuttons. Its outputs are used by the control circuitry to properly configure the system for the selected mode. Further, when U11B transitions from the "unlocked" state to the "locked" state, it triggers U12. The resulting pulse causes U6, U7 and U8 to asynchronously shift state to "8", "9" and "high" respectively. This establishes the desired, known state for an orderly transition from the unlocked to locked mode.

The 1.02-second gating pulses required in the locked mode are generated by U11A.

C. CONTROL CIRCUIT

Figure 25 is a diagram of the system control circuit. It routes the various sequencing pulses and oscillator outputs to the appropriate inputs of the counters and latches. Provision is made for programming the system for a particular hetrodyne scheme and for the orderly transition from the unlocked to the locked mode.

Figure 25
Control Circuit



1. Unlocked Mode

Referring to Figures 20 and 25, the control circuitry, in the unlocked mode, functions as follows. U13 is a dual, four-input multiplexor which selects the secondary oscillators and provides, via its chip enable input, the one-second gate for the secondary counter measurement period. The oscillators are selected in the sequence 0-1-2-3-0-1-2-etc. Starting with the "zero" inputs, the secondary oscillators are connected to the UP-UL or DN-UL side, depending upon whether the oscillator is to be counted up or down in the unlocked mode. The other input with the same number is grounded to provide noise immunity. The UP-UL inputs are routed to the secondary counter UP input and the DN-UL inputs are routed to the secondary counter DN input via U14, a quad two-input multiplexor.

U18B, U18C and U20C provide the count interval gating and input selection for the primary counter. Either L or UL signals are connected to the input of U20C to program the primary counter to count down or up in the unlocked mode.

U15A and U15B form the "current secondary oscillator" counter. Ten milliseconds after the end of a one-second measurement period, pulse P1 advances the count to select the next secondary oscillator. At 20 ms, pulse P2 enables U18A, the "end of secondary update cycle" decoder. The outputs of U15A and U15B are jumpered to the inputs of U18A as appropriate to program the system for the proper number

of secondary oscillators. If the secondary update cycle is not complete, U16B and U16C inhibit secondary counter clear and secondary latch load. U14 inhibits secondary counter load at all times when the system is in the unlocked mode. At 40 ms, pulse P4 is gated by U16D to load the primary latch, and at 80 ms, pulse P8, buffered by U20B, causes a primary counter load. The system is now ready to count the next secondary oscillator.

If, after the next count, the secondary update cycle is complete, U18A detects the condition at the time of P2 and U15A and U15B reset to zero. U17B detects these zero states and enables U16B and U16C. At the time of P4 both the primary and secondary latches are loaded by pulses gated by U16C and U16D. At the time of P6 the secondary counter is cleared via U16B and at the time of P8 the primary counter is loaded as previously described.

U17C is the integrator arming latch and is held in the "disarmed" state at all times while the system is in the unlocked mode.

2. Locked Mode

In the locked mode the direction of counts is reversed by U14, U18 and U20. The secondary counter load function is enabled by U14 and the primary latch load function is disabled by U16D. U14 also extends the primary count interval to 1.02 seconds.

Referring to Figures 21, 23 and 25, when the locked mode is entered a pulse from U12 forces the timing circuit

to the beginning of a P8 pulse period. This pulse also resets U15A and U15B, via U17A, to zero, which in turn enables U16A via U17B. As a result there is an immediate loading of the secondary counter and the system is ready to start the first count in the locked mode. Note that U17C is still in the "unarmed" state and will remain in that state until the end of the first secondary update cycle. Except as noted above, the circuit operates in the same manner as in the unlocked mode.

D. STEERING LOGIC

The steering logic circuit used in the system is shown in Figure 26. This is the same circuit as shown in Figure 17 except that provision has been made for ensuring that the "phase detector", U21, begins locked mode operation in the correct state, i.e., both outputs inactive (high). Additionally, the borrow and carry outputs of the primary counter are OR'ed together so that no jumper is required to program this particular portion of the system for a given hetrodyne scheme.

Without the additional circuitry it would be possible for one of U21's outputs to be active when the locked mode is entered and the integrator is armed. If this happened, pulses from the VFO would immediately and erroneously be gated to the integrator causing it to "run away."

Since the output states of U21 are a function of the sequence of input transitions, a circuit to cause U21 to assume a desired state, regardless of its current state,

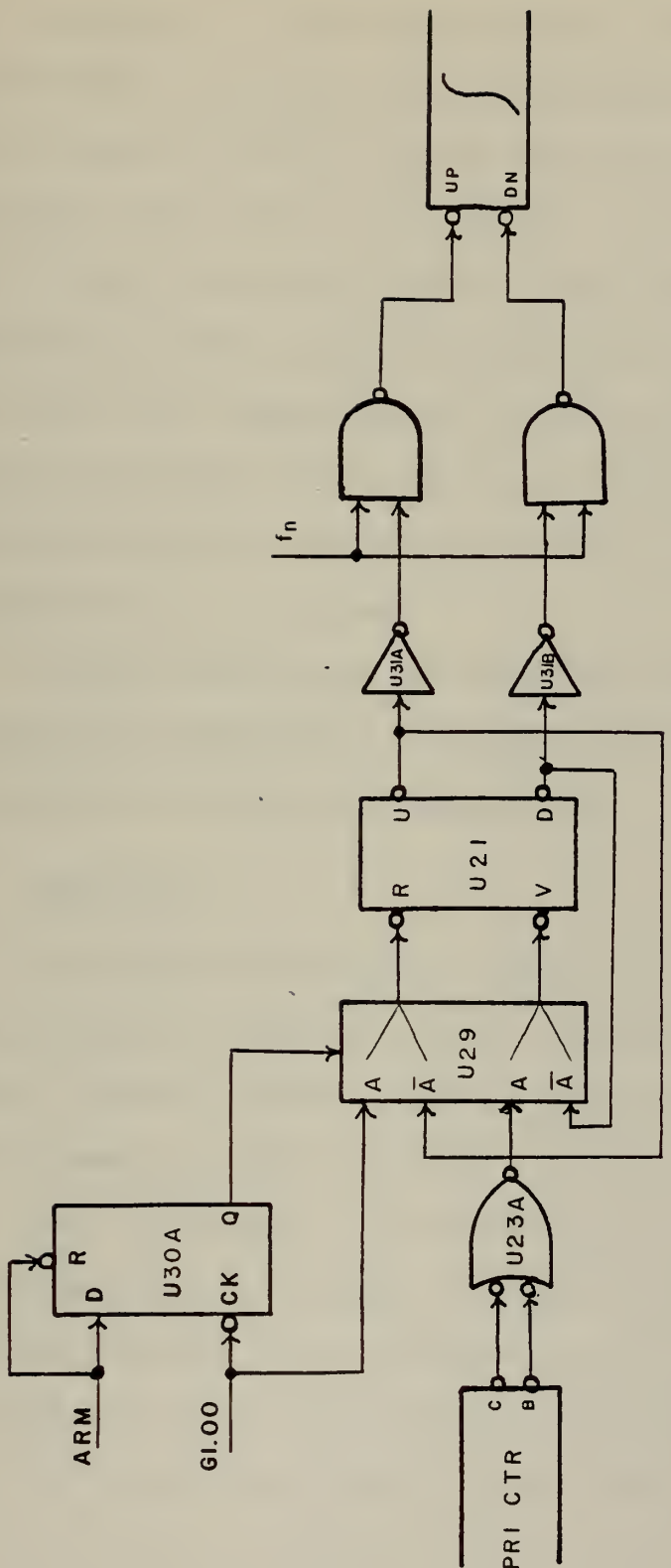


Figure 26 Steering Logic

must provide a sequence of transitions to the input of U21 as a function of its output states. U29, half of a quad-2-input multiplexor, accomplishes the task of forcing both outputs of U21 to their inactive state by creating feedback paths from the U output to the V input and from the D output to the R input. These paths exist, under the control of U30A, while the system is in the unlocked mode and until the beginning of the first count interval of the second secondary update cycle in the locked mode. This assures that any transients caused by U29 occur when the integrator is not armed.

In the locked mode U29 switches the circuit to a configuration essentially the same as in Figure 17 and it functions as previously described.

E. INTEGRATOR

The system integrator, shown in Figure 27, uses the up-down counter scheme previously described. U25 through U28 form a 16-bit counter. In the unlocked mode the R-S flip-flop formed by U24A and U24B is held in the "set" state by the low, ARM signal. As a result, the load input of U28 and the reset inputs of U25, U26 and U27 are held active. This further results in the counter being forced into a null (midrange) state with the most significant bit set to one and all other bits reset to zero. The counter remains in this state at all times while in the unlocked mode.

At the time of P4 just prior to the first measurement period of the second secondary update cycle in the locked

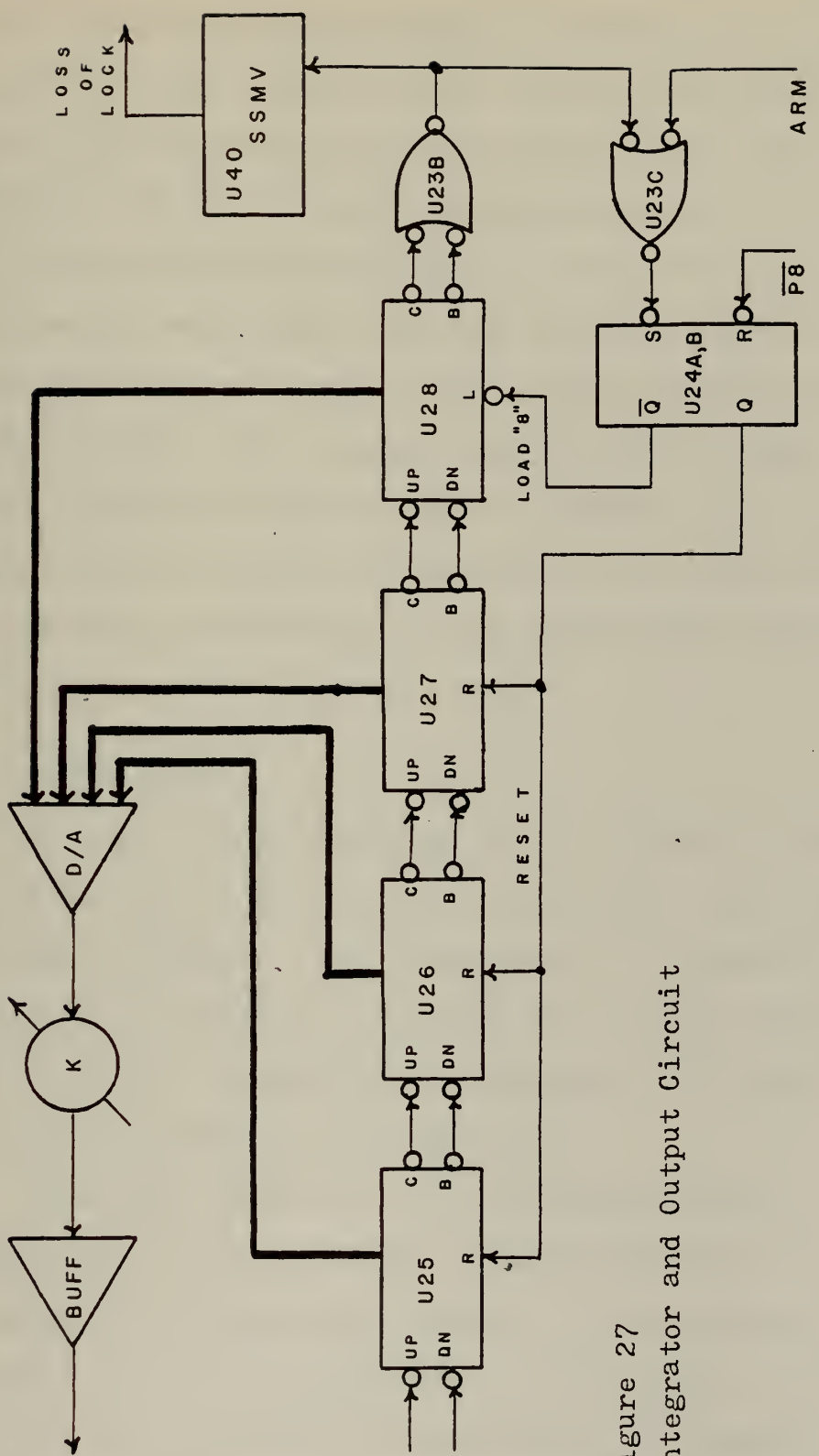


Figure 27
Integrator and Output Circuit

mode, the ARM signal goes high, allowing the subsequent P8 signal to reset U24A and U24B. This removes the load and reset signals from the counter which is now ready to integrate the first valid error measurement.

Any overflow or underflow of the counter is detected by U23B which, via U23C, sets U24A and U24B which in turn resets the counter to null. The subsequent $\overline{P8}$ pulse resets U24A and U24B. The signal from U23B also triggers U40 which flashes a "loss of lock" indicator. By resetting null after an overflow or underflow, the system has a better chance of recovering for an uncorrected frequency error at the edge of the system's range.

F. PROGRAMMING

An important design goal was to develop a system which could be used with equipments employing a wide variety of hetrodyne schemes. The final design is capable of controlling an equipment employing up to five oscillators. This capacity is sufficient for almost all existing high-frequency communications equipment.

Since the connection to an equipment would be semi-permanent or even permanent, programming the system is accomplished by connecting jumpers in the control circuitry (Figure 25). The programming for the number of secondary oscillators involved is accomplished by jumpering the appropriate outputs of U15A and U15B to the decode inputs of U18A. The outputs selected are those which are high when the counter formed by U15A and U15B contain the

binary number equivalent to the total number of secondary oscillators. For example, if there are two secondary oscillators, the $\overline{Q}$ output of U15A and the Q output of U15B are selected. If there are four secondary oscillators the jumpers may be ommitted or connected to the $\overline{Q}$ outputs.

The direction of count for each of the secondary oscillators is programmed by connecting the signal from a particular oscillator to the appropriate input of U13. The first oscillator to be counted in each secondary update cycle is connected to a "zero" input. If this oscillator is to be counted down in the unlocked mode, its signal is connected to the DN-UL side of U13. Conversely, if it is to be counted up it is connected to the UP-UL side. The remaining secondary oscillators are similarly connected to the inputs in ascending numerical order. All unused inputs are jumpered to ground to preserve noise immunity.

The direction of count for the primary oscillator is programmed by jumpering the input of U20C to UL or L output of U11B (Figure 23) as appropriate. If the count is up in the unlocked mode, the UL output is selected. Conversely, if the count is up in the locked mode the L output is selected.

A total of ten jumpers is required to program the system for a particular hetrodyne scheme. Because of the anticipated low frequency of changes in the programming, it was felt that the inclusion of switches or additional electronic circuitry to accomplish this programming was not justified.

G. EQUIPMENT MODIFICATIONS AND INTERFACING

The communications equipment to be controlled must be modified in two respects. First, the outputs of the oscillators must be brought out of the equipment for connection to the AFC system. Secondly, the primary oscillator (master oscillator, VFO, etc.) must be modified to be voltage controllable. These modifications must be made without degrading the equipment's performance. How these modifications are made depend upon a particular equipment's design and no all-inclusive scheme is possible.

Connection to an R-390 receiver for system testing was particularly simple. The oscillator outputs are connected to their associated mixers by coaxial cable and connectors. Bringing out the signals involved simply inserting "T" connectors in series with the cables. The VFO is a sealed unit. Even so, it was possible to make this unit voltage controllable by connecting a varactor diode via a short lead wrapped around a tube pin. These connections actually didn't involve "modifying" the receiver and probably wouldn't be satisfactory for a permanent installation. Connection to other equipments could be much more difficult and could require both mechanical and electrical modifications.

There are two corresponding interface requirements in the AFC system. The first is circuits to change the oscillator output signals into logic levels for counting. In the prototype system simple MOS transistor amplifiers were used. Additionally, the overall loop gain must be set for

proper system performance. In the prototype this was accomplished by connecting the output of the D/A converter to an operational amplifier (configured for a gain of 10) via a potentiometer. The potentiometer is adjusted for the desired shift in primary oscillator frequency for a given change in D/A converter output voltage.

IV. EVALUATION AND CONCLUSIONS

The testing and evaluation of the AFC system prototype was conducted in two phases. The first consisted of checking the operation of the digital circuitry by simulating the communications equipment with laboratory signal generators. The second phase consisted of connecting the system to two different communications receivers and verifying proper system operation.

A. INITIAL TESTS

The setup shown in Figure 28 was connected to check overall system operation. The signal generators were set to various frequencies in the 0.5 to 10 MHz range. With the system in the unlocked mode it was confirmed that the system accurately displayed the sum or difference frequency. Then, with the control loop open, the system was placed in the locked mode. The frequency of one of the oscillators was then changed slightly. It was observed that the frequency displayed remained unchanged and that the control voltage step-ramped at a rate proportional to the created "error." It was also observed that the control voltage properly reset to "null" after an overflow or underflow of the integrator. This was repeated for several combinations of frequencies. The above was repeated with the control loop closed for several different values of loop gain. The system performed as predicted. The system was stable

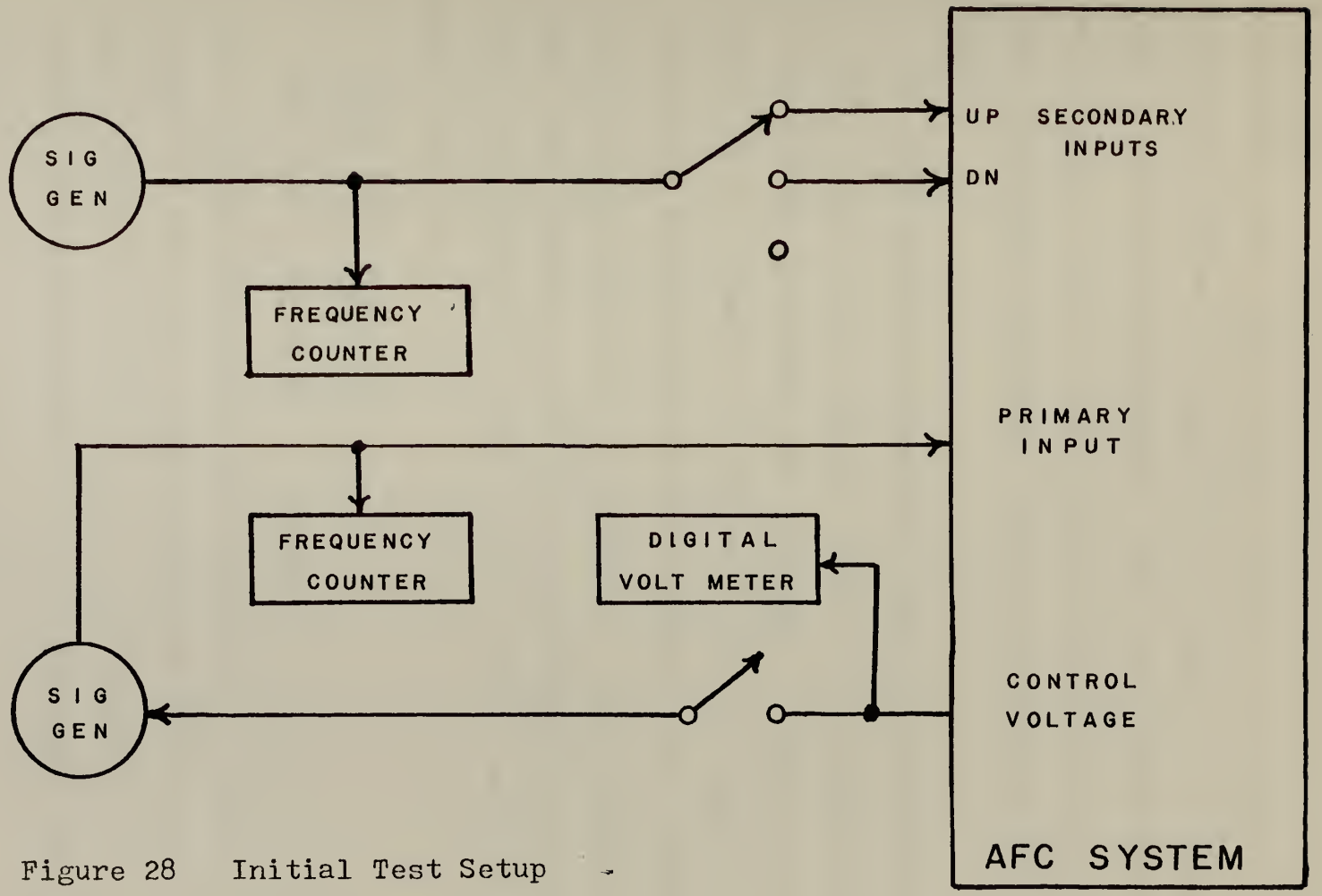


Figure 28 Initial Test Setup

for values of loop gain in the range $0<k<2$. For $k>1.5$ the effects of quantization became pronounced and there were noticeable "limit cycle" effects. For $k\leq 1.0$, recovery from step changes in frequency were smooth and quantization effects were not discernable. For k very near one the system recovered from a step change in frequency within two or three measurement periods, even for relatively large step errors.

The only problem discovered during these initial tests was that if the error exceeds 2.0% of the primary oscillator frequency the system may "runaway." This is due to the fact that the primary counter may not reach zero in the 1.02-second locked mode counting period. As a result, the steering logic gets out of sequence. This problem is not significant because an error of this magnitude is also well beyond the correction range of the system, even with loop gains near two.

B. TESTS WITH RECEIVERS

The test setup shown in Figure 29 was used to determine actual system performance when connected to communications equipment. The first receiver used was an SX-130, a very simple single conversion general coverage receiver. It was selected as being representative of the "worst case" the system would have to contend with.

The system was normally interfaced to the receiver except that the control voltage was monitored with a digital voltmeter. A frequency counter was connected to the audio

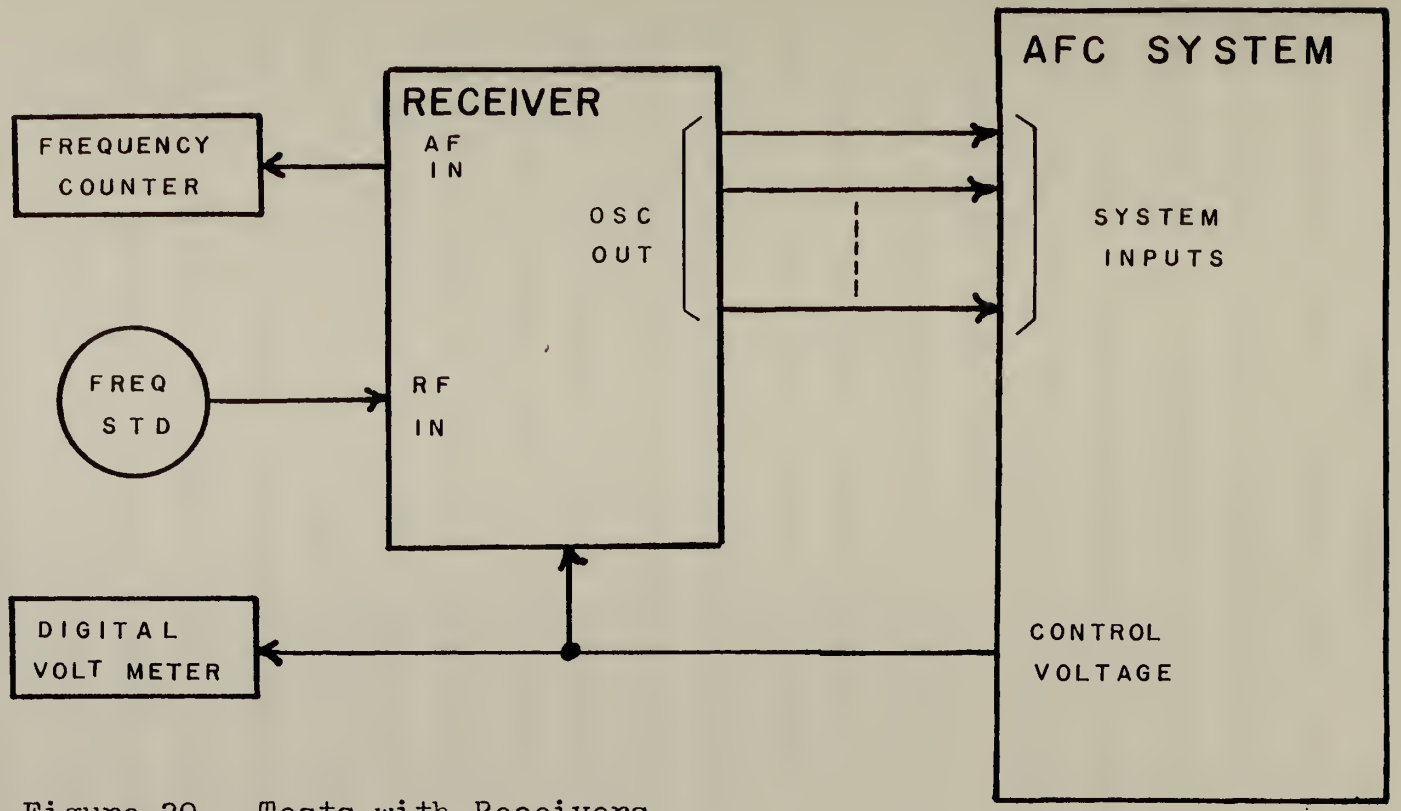
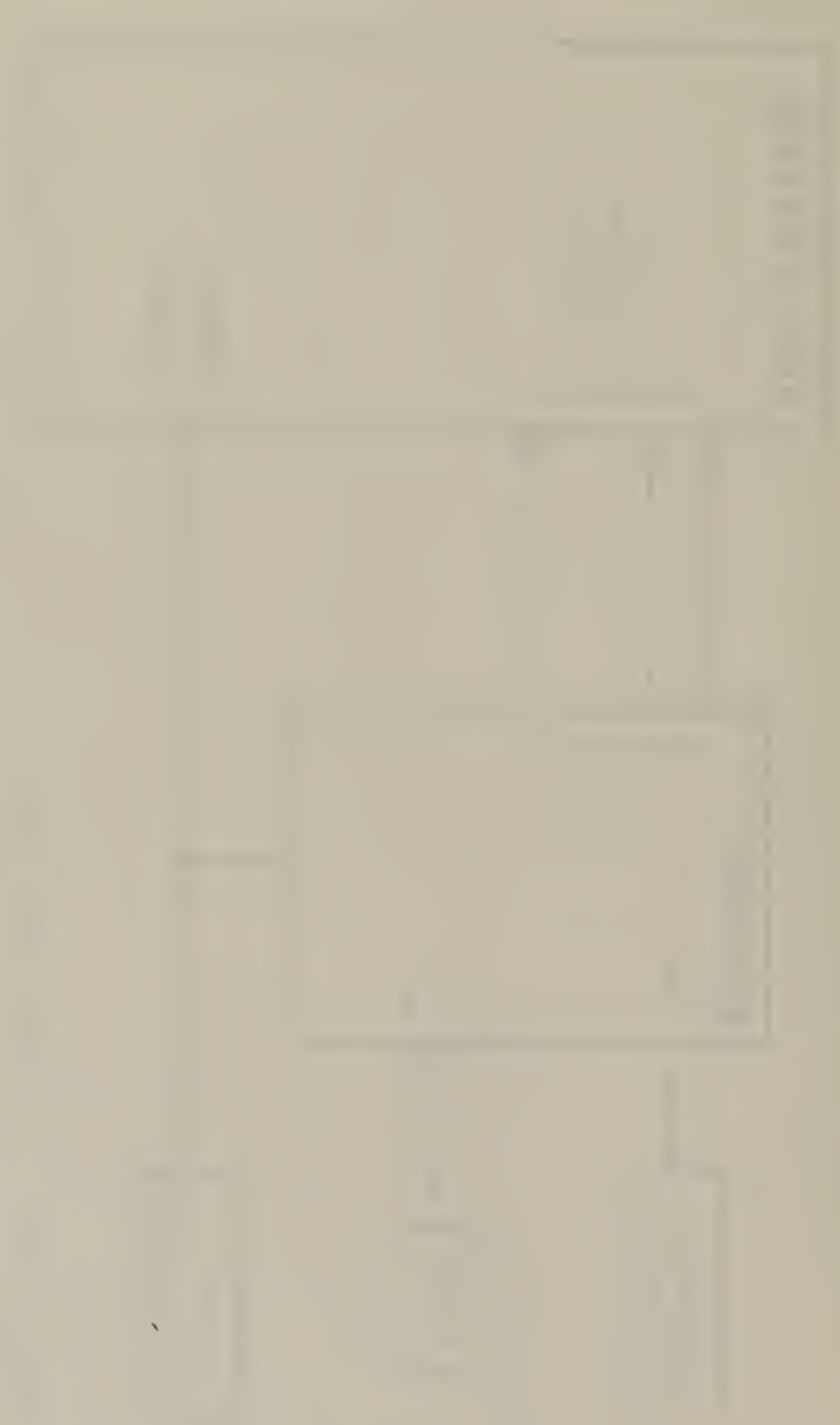


Figure 29 Tests with Receivers



output and a frequency standard connected to the RF input. The standards used were receiving WWV off the air and a crystal calibrator.

With the BFO on, the system in the unlocked mode, the receiver was tuned to the frequency standard such that the beat frequency output was approximately 1.0 KHz. It was confirmed that, depending upon the side of zero beat to which tuned, the system accurately displayed the sum or difference of the frequency of the standard and the frequency of the audio output.

The uncontrolled frequency stability was observed to be as follows. With the receiver tuned to 5.0 MHz there were, from second to second, random variations of up to 15 Hz in both counter and system measured frequency. In addition, after warmup there was an overall drift in frequency at rates up to 1 KHz per minute. Mechanical stability was checked by striking the receiver smartly with the fist. Frequency jumps up to 500 Hz were observed.

When placed in the locked mode with the loop gain set to about 0.8 the frequency stability was observed to be as follows. The second-to-second random variations in frequency remained about the same. There was no detectable net drift. Any steady state drift errors were masked by the random variations. The system recovered from step changes in frequency caused by striking the receiver to within the range of the random variations within three to five seconds.

When the loop gain was increased to over one an increase was noted in the magnitude of the random variations. No improvement in performance was noted except step recovery for values very near one.

A serious problem was encountered when interfacing the system to this receiver. The tuning rate, especially from band to band, is extremely non-linear. As a result a "constant gain" VCO conversion was not possible. If the system were to be used with this type of receiver provision would have to be made for correcting loop gain as a function of operating frequency.

The above tests were repeated with the system connected to an R-390A receiver. The uncontrolled frequency stability was observed to be as follows. With the receiver tuned to 5.0 MHz, there were no discernable random variations in frequency. The maximum drift observed after warmup was about 75 Hz in a one-hour period. The maximum frequency jump due to striking the receiver was about 10 Hz.

When placed in the locked mode with the loop gain set to 0.3 the frequency stability was observed to be as follows. No quantization effects were noted and the second-to-second frequency measurements remained constant. In a one-hour period there was no detectable drift and the steady state drift error was less than 1 Hz. The system recovered to within 1 Hz after being struck in less than five seconds. It recovered from being detuned 1 KHz in about 15 seconds.

The tests were repeated on different bands with similar results. When repeated with increased loop gain the

recovery from step frequency changes improved as expected but quantization effects became noticeable for gains greater than about 0.6

C. EVALUATION OF TESTS

The system performance was very close to that predicted by the model. When used with equipment with very poor stability the effects of drift and large frequency jumps can be corrected but short-term stability is not improved. This is consistent with the fact that the design was based on the assumption of good short-term stability.

When used with equipment with very good short-term stability the effects of long-term drift can be essentially eliminated without inducing any unwanted side effects. To accomplish this a relatively low value of loop gain must be used. This results in undramatic recovery from step changes in frequency, but in practice such errors should be rare.

D. CONCLUSIONS

The performance objectives of the design were realized but it required a greater system complexity than was desired. To be truly practical the system would have to be further simplified or the design realized with less expensive components.

A great majority of the circuitry is associated with measuring the true operating frequency and in the digital display. A reduced system which stabilized a single

oscillator and had no frequency display would require only about one-third the circuitry of the full system.

Some minor economics could be realized if the system were designed to service a single hetrodyne scheme, but the loss in flexibility would probably make this undesirable.

Large scale integrated circuits appropriate for use in this system are now becoming available and their cost will soon be low enough to make a significantly less expensive design possible. If enough of the systems were to be produced (in the thousands) large scale integrated circuits specifically designed for this application would become a possibility.

The system design as it stands demonstrates that such a device can greatly improve the frequency accuracy and long-term stability of existing conventionally-tuned communications equipment. Whether or not this can be done in a cost effective manner has not been established.

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